

FIG. 1

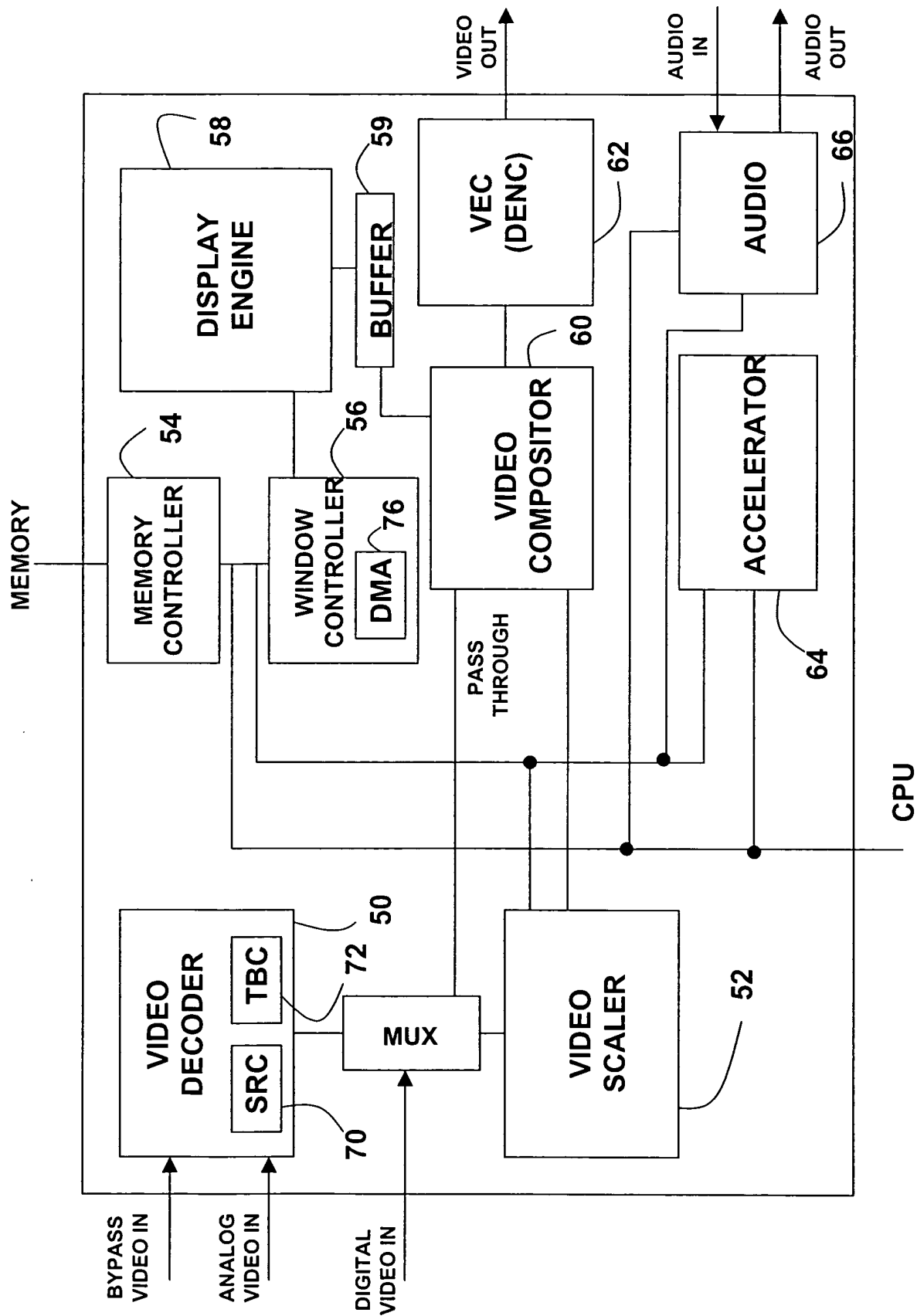


FIG. 2

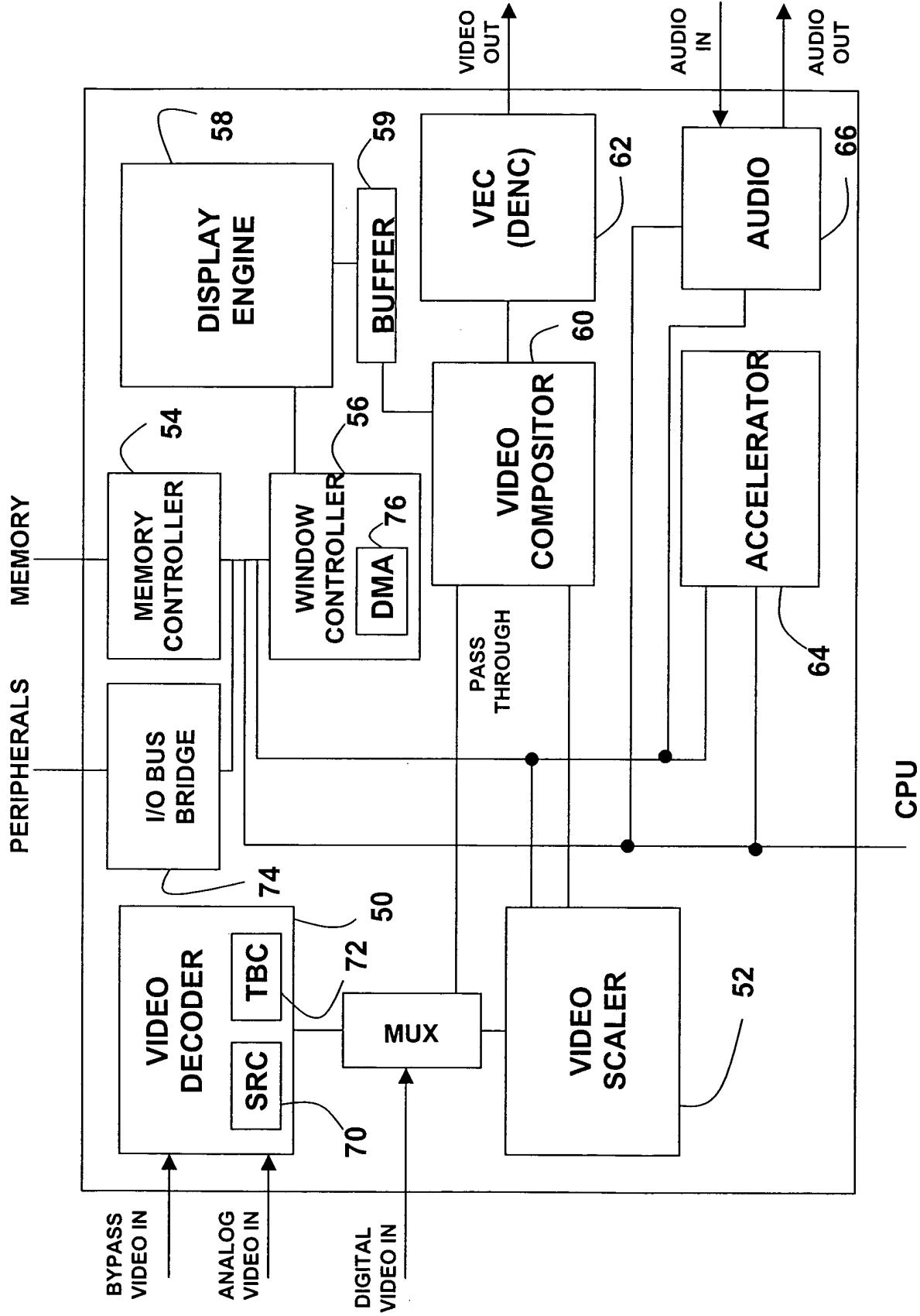


FIG. 3

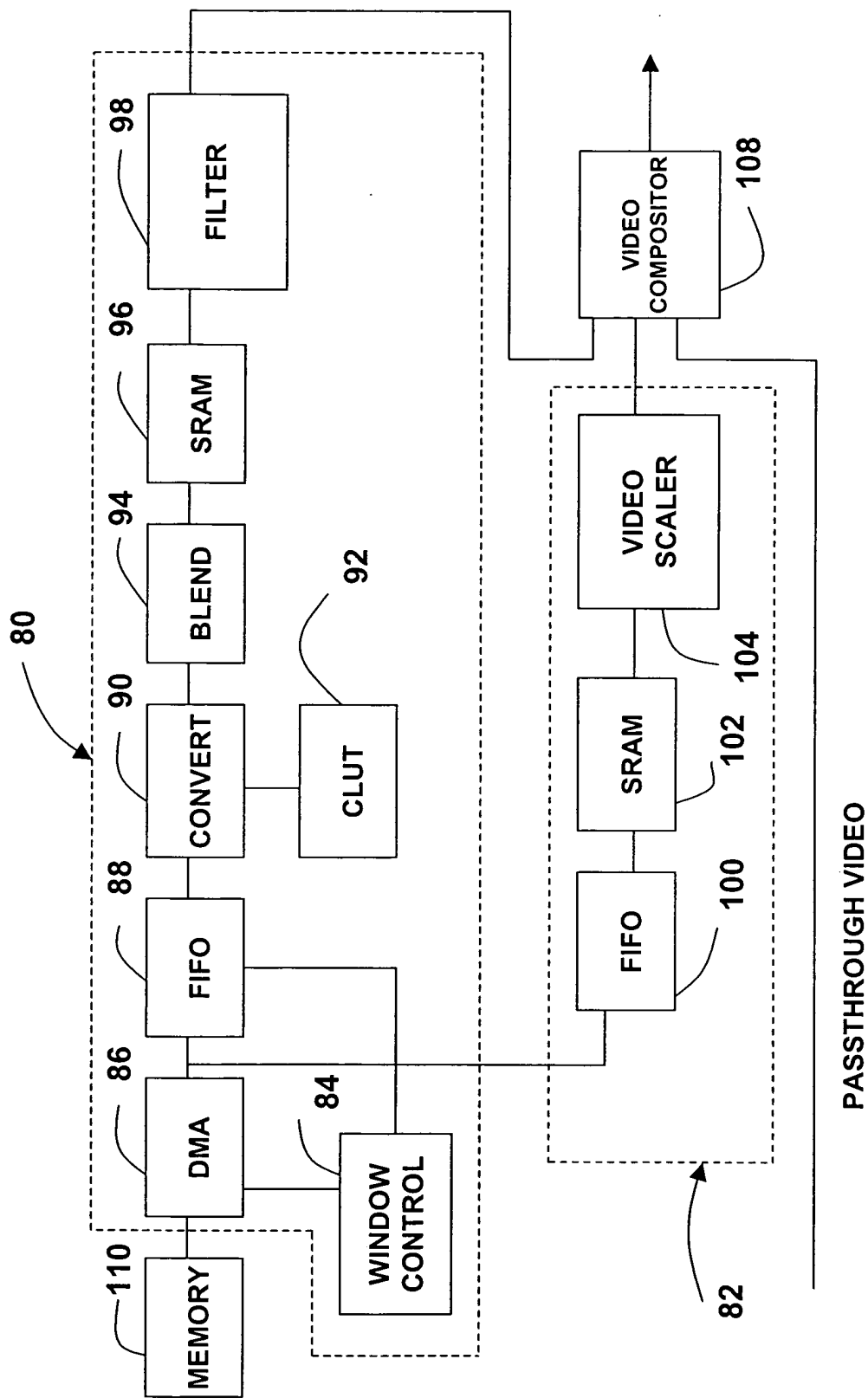
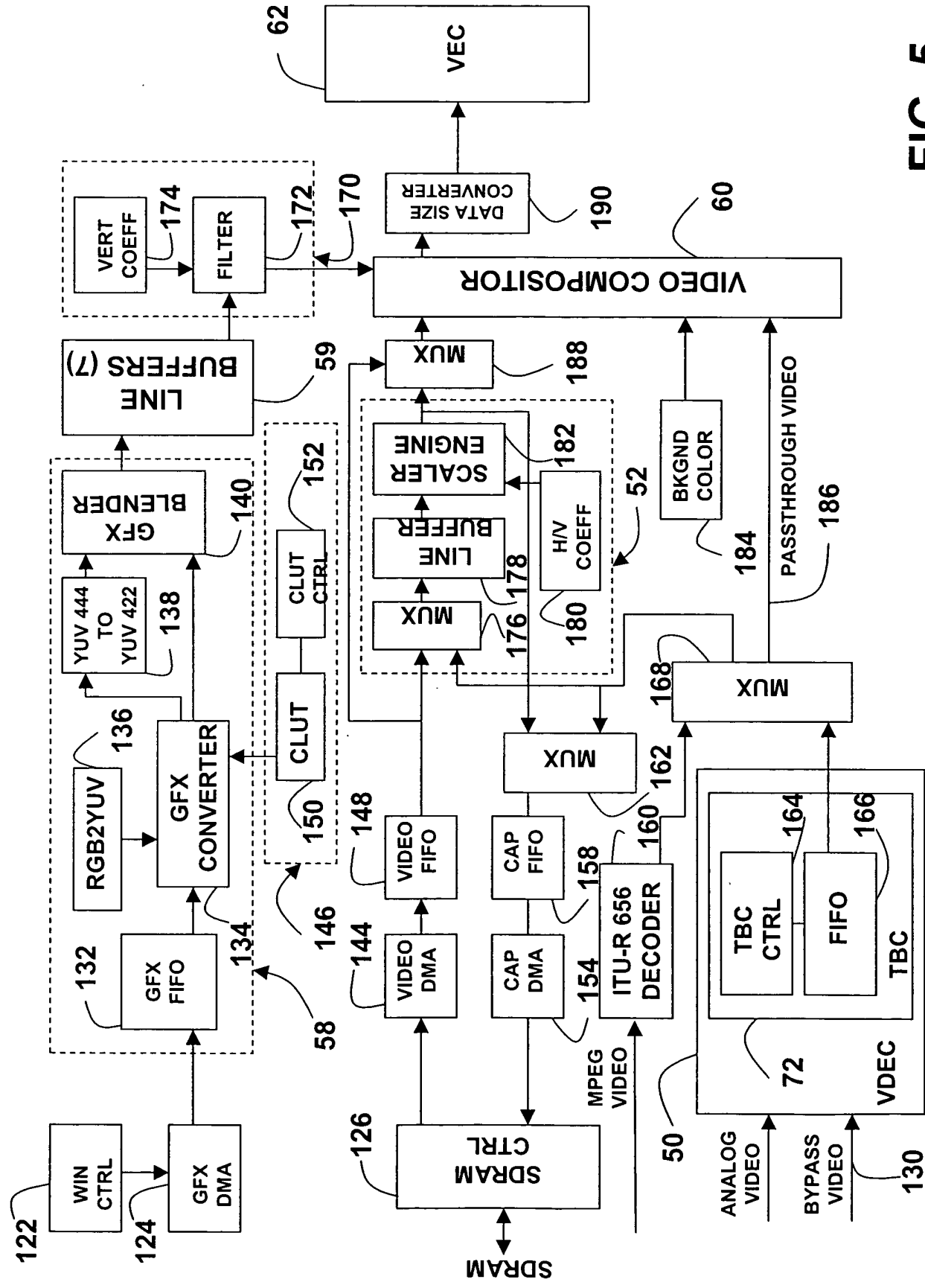


FIG. 4



**FIG. 5**

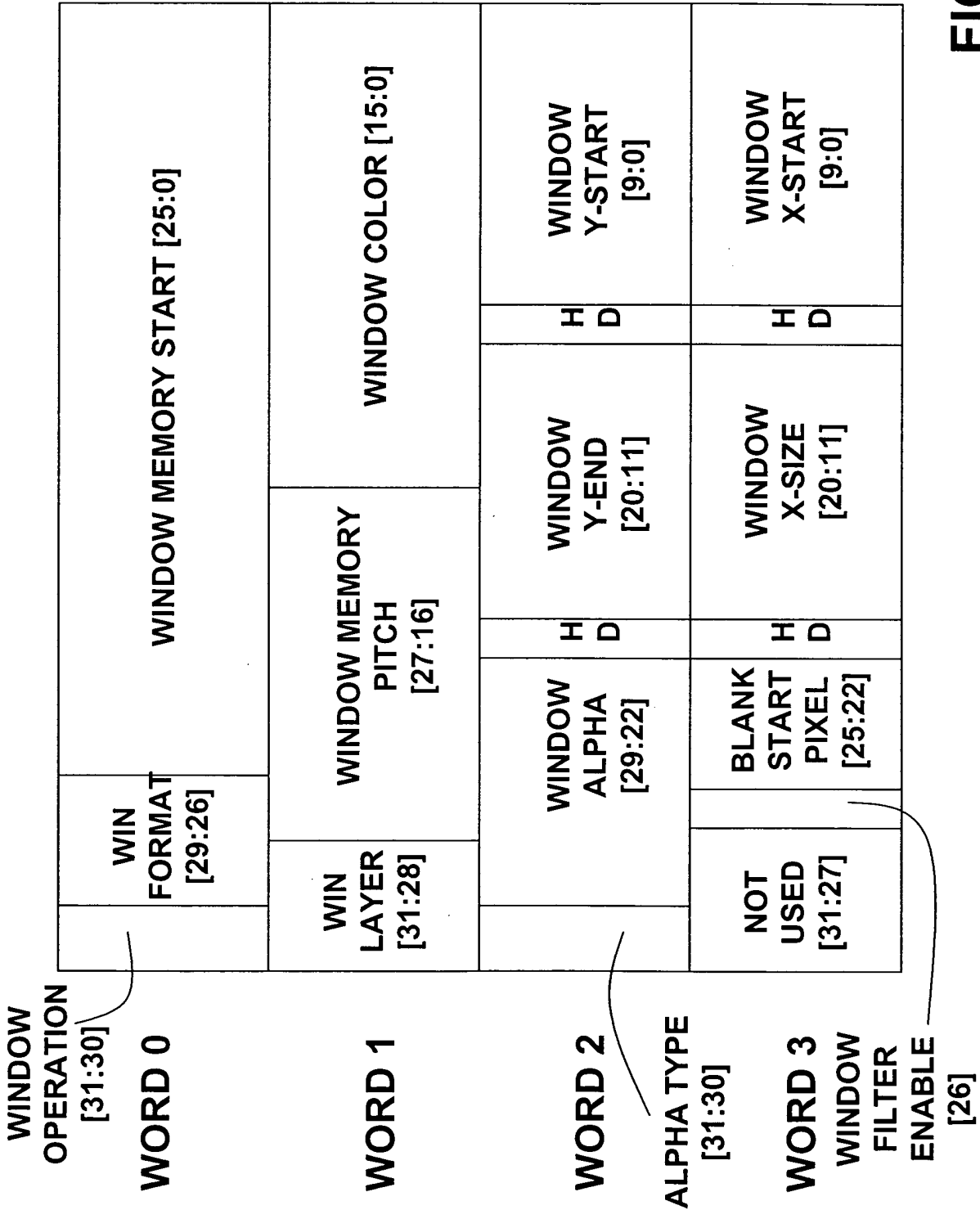


FIG. 6

The diagram illustrates the processing of window descriptors. At the top, eight window descriptors (WD0 to WD7) are shown, each with parameters labeled 300a through 300h. These parameters are fed into a multiplexer (MUX) and a sorting unit (304). The MUX selects the 'smallest WD parameters' (302) based on the sorting unit's output. The selected parameters are then processed by a DMA unit (306), which handles 'assemble header and request memory data'. The DMA unit is connected to a 'memory controller' at the bottom. The output of the DMA unit is 'WD header, GFX data', which is then passed through a 'GFX FIFO' (308) before being sent to the 'GFX - DISP' output.

FIG. 7

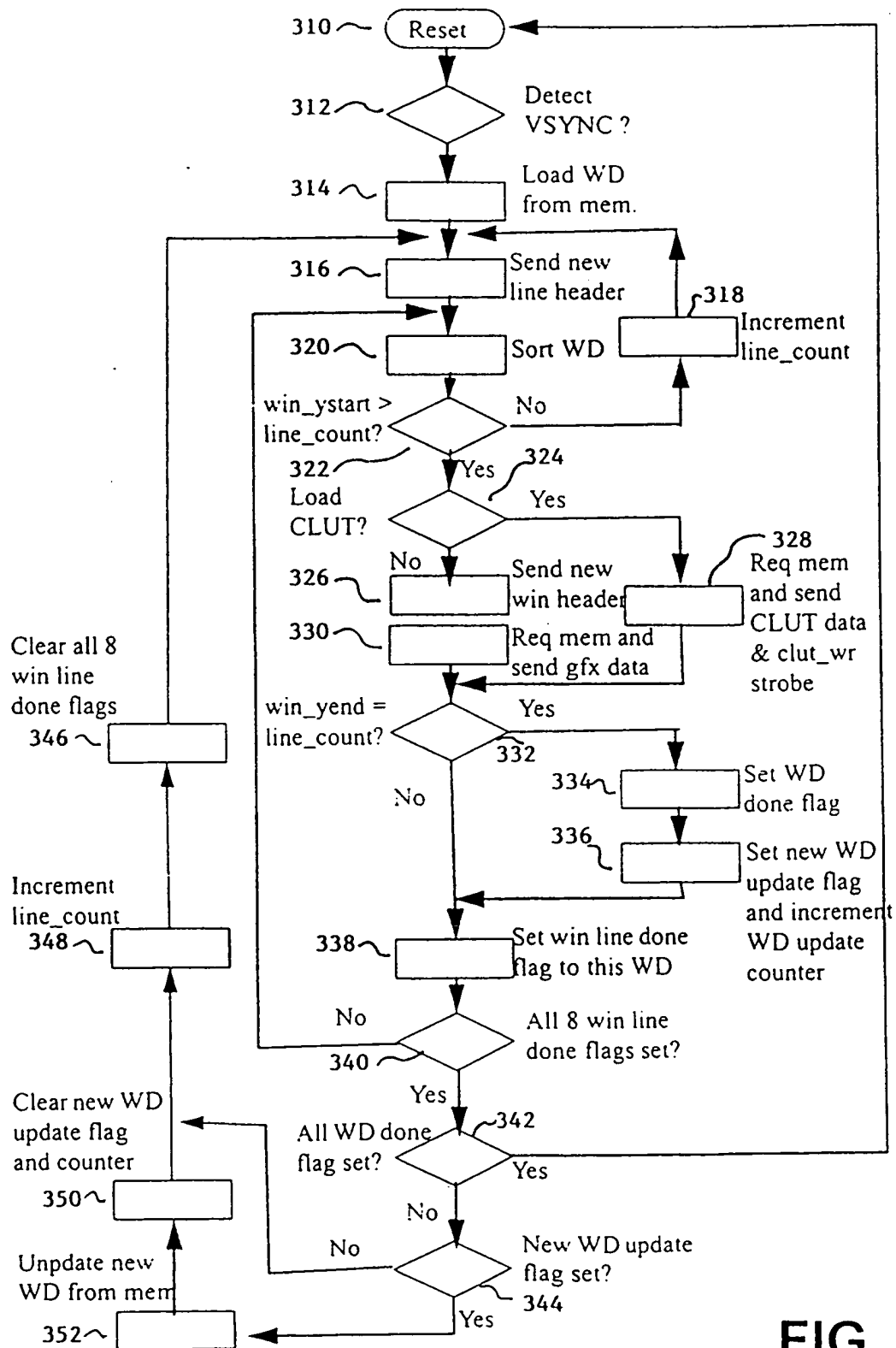
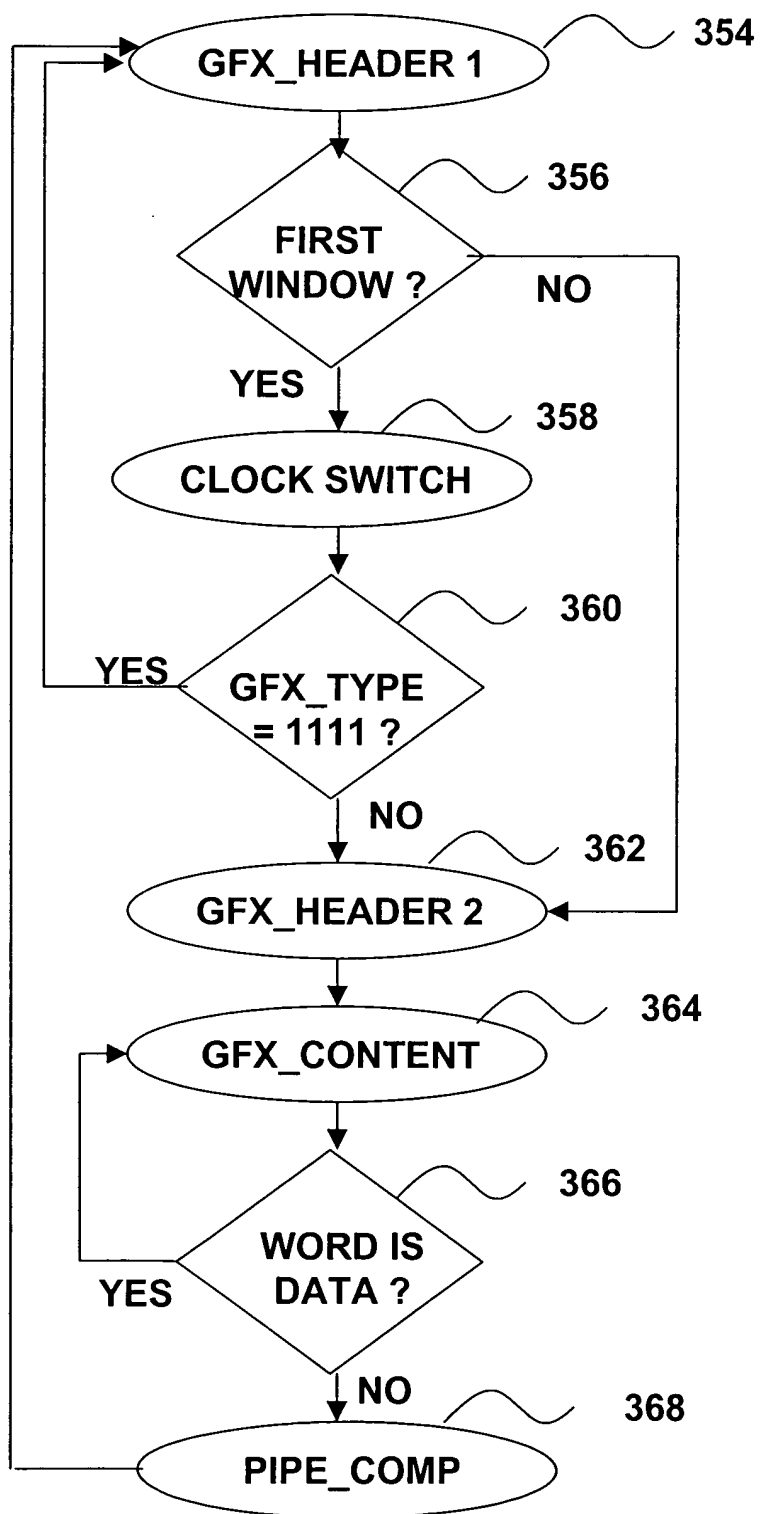


FIG. 8





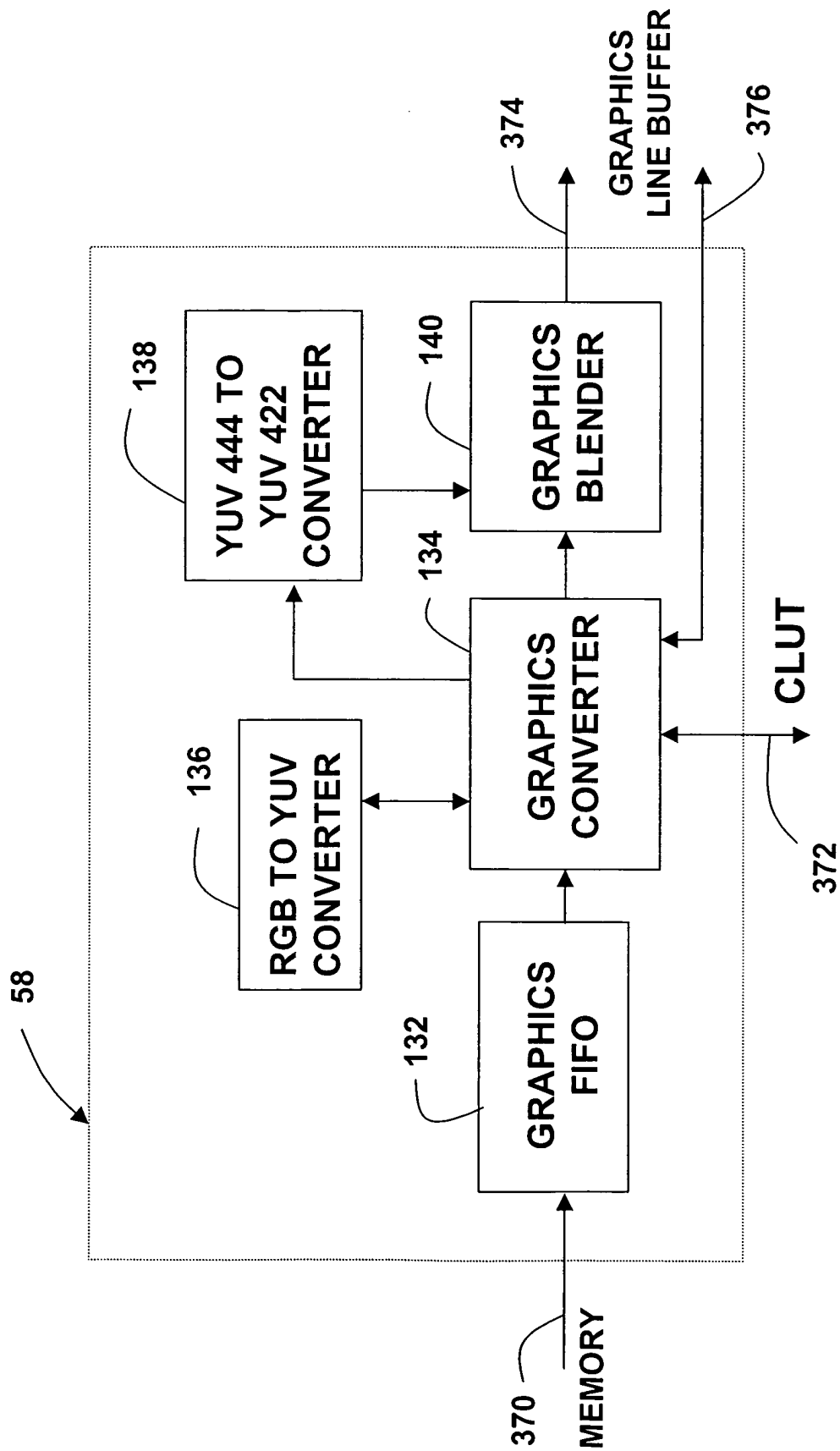


FIG. 10

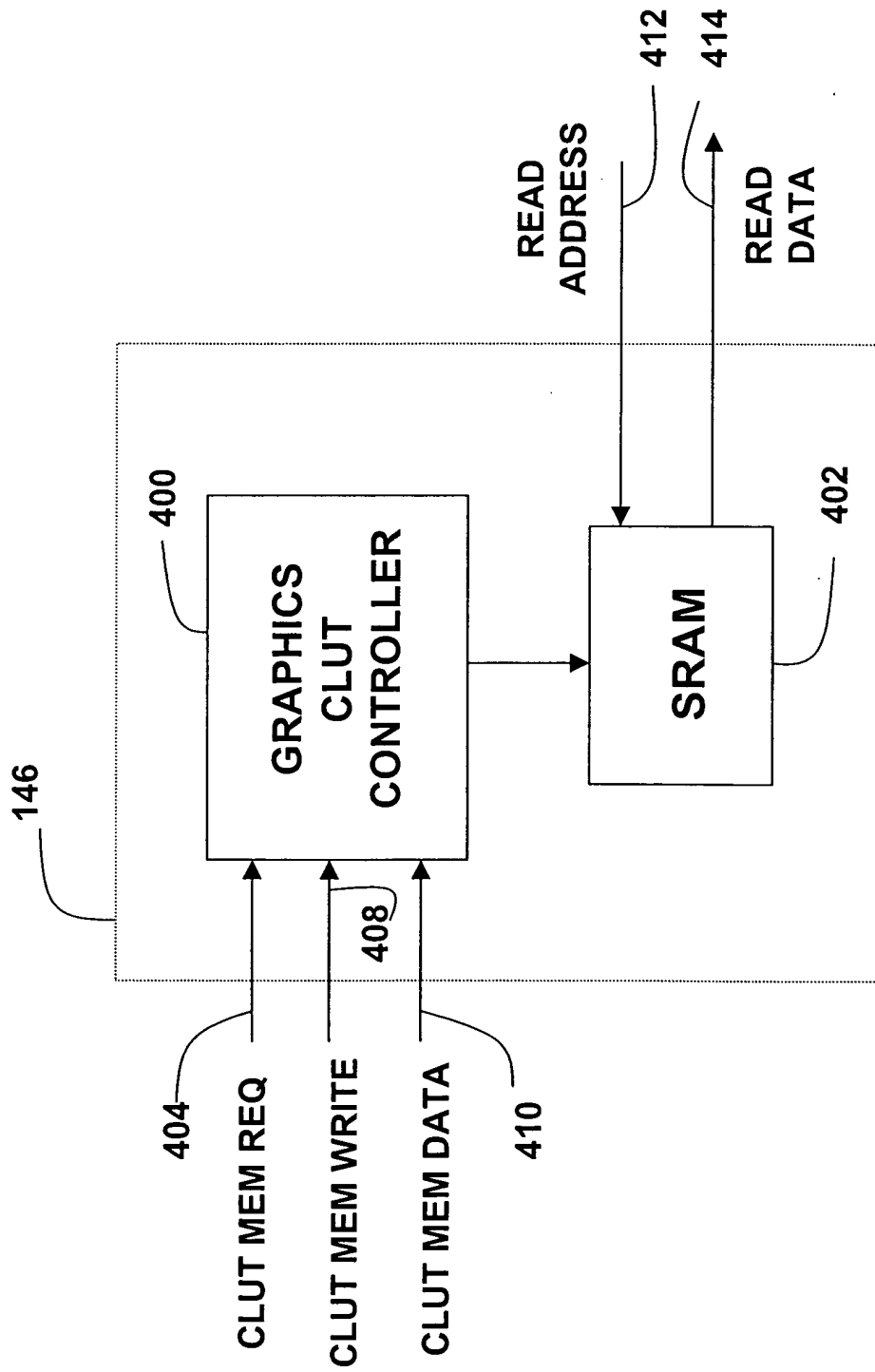
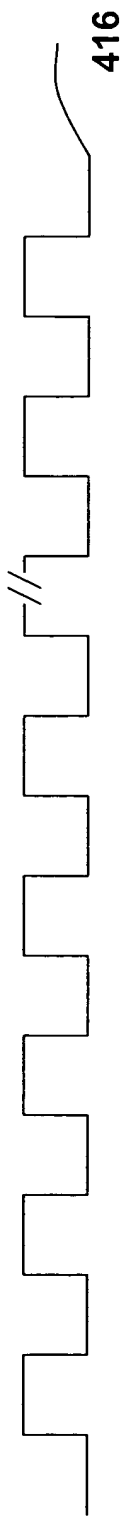


FIG. 11

MEMORY CLOCK



CLUT MEMORY REQUEST



CLUT MEMORY WRITE



CLUT MEMORY DATA



FIG. 12

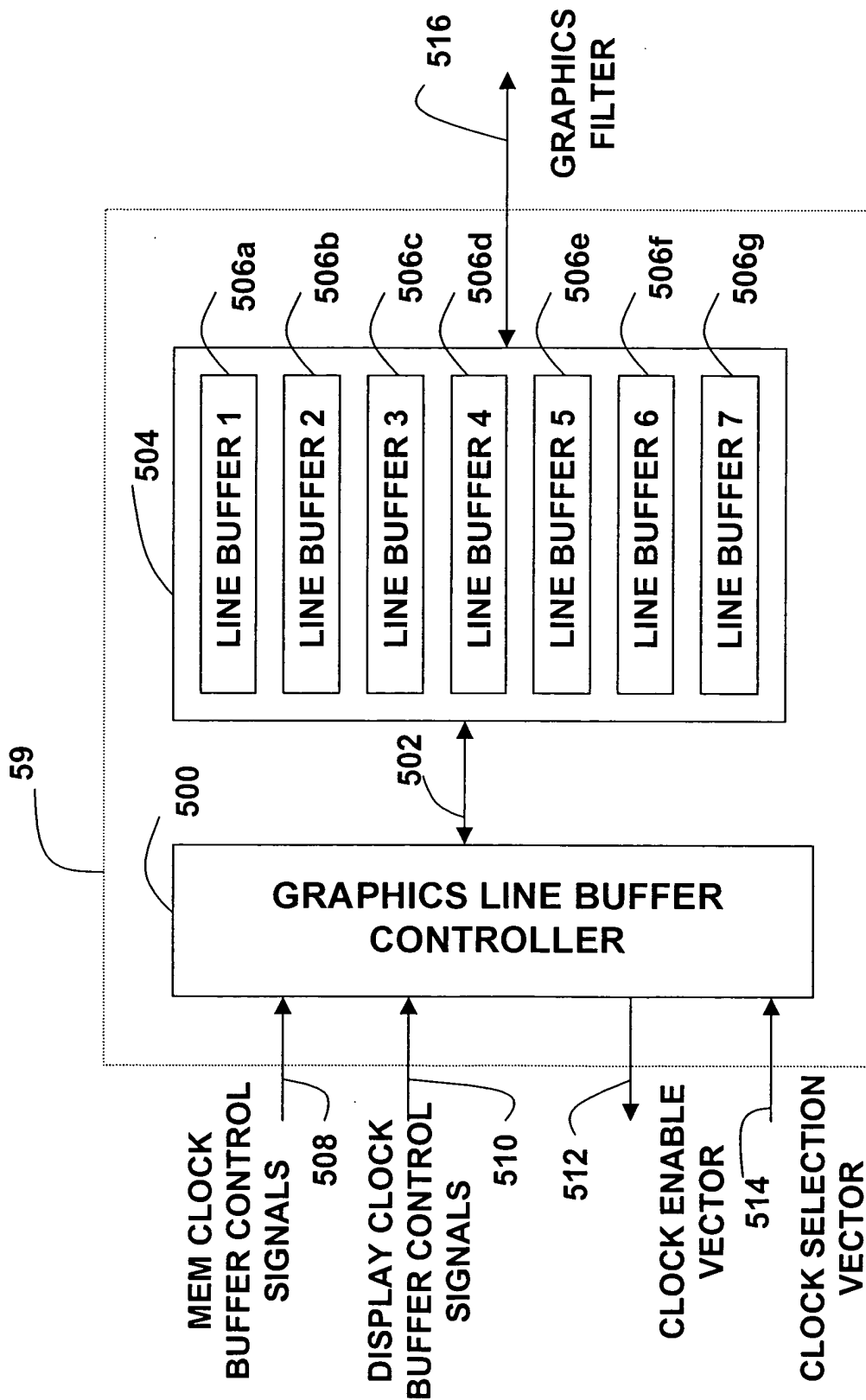
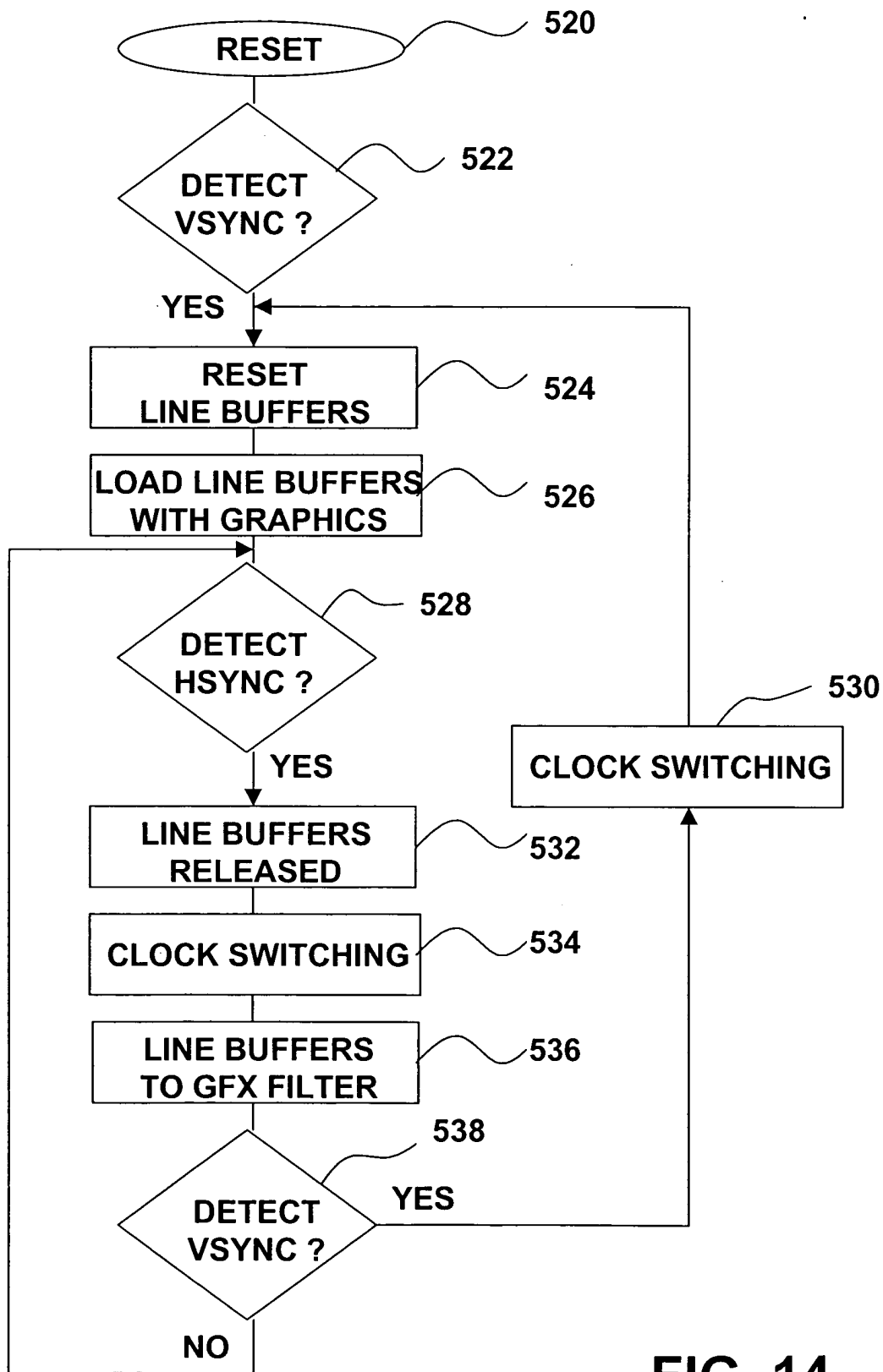


FIG. 13



**FIG. 14**

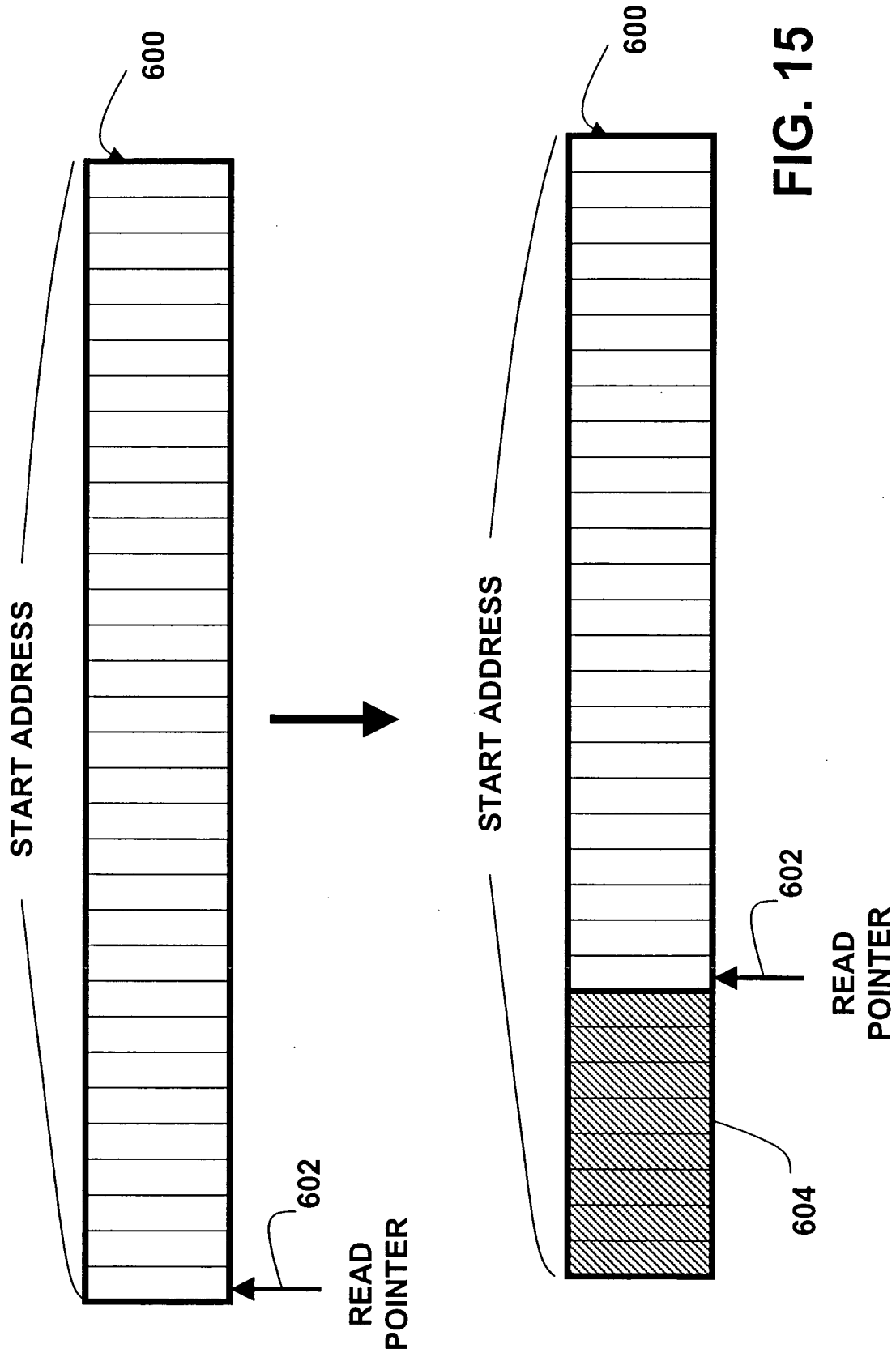


FIG. 15

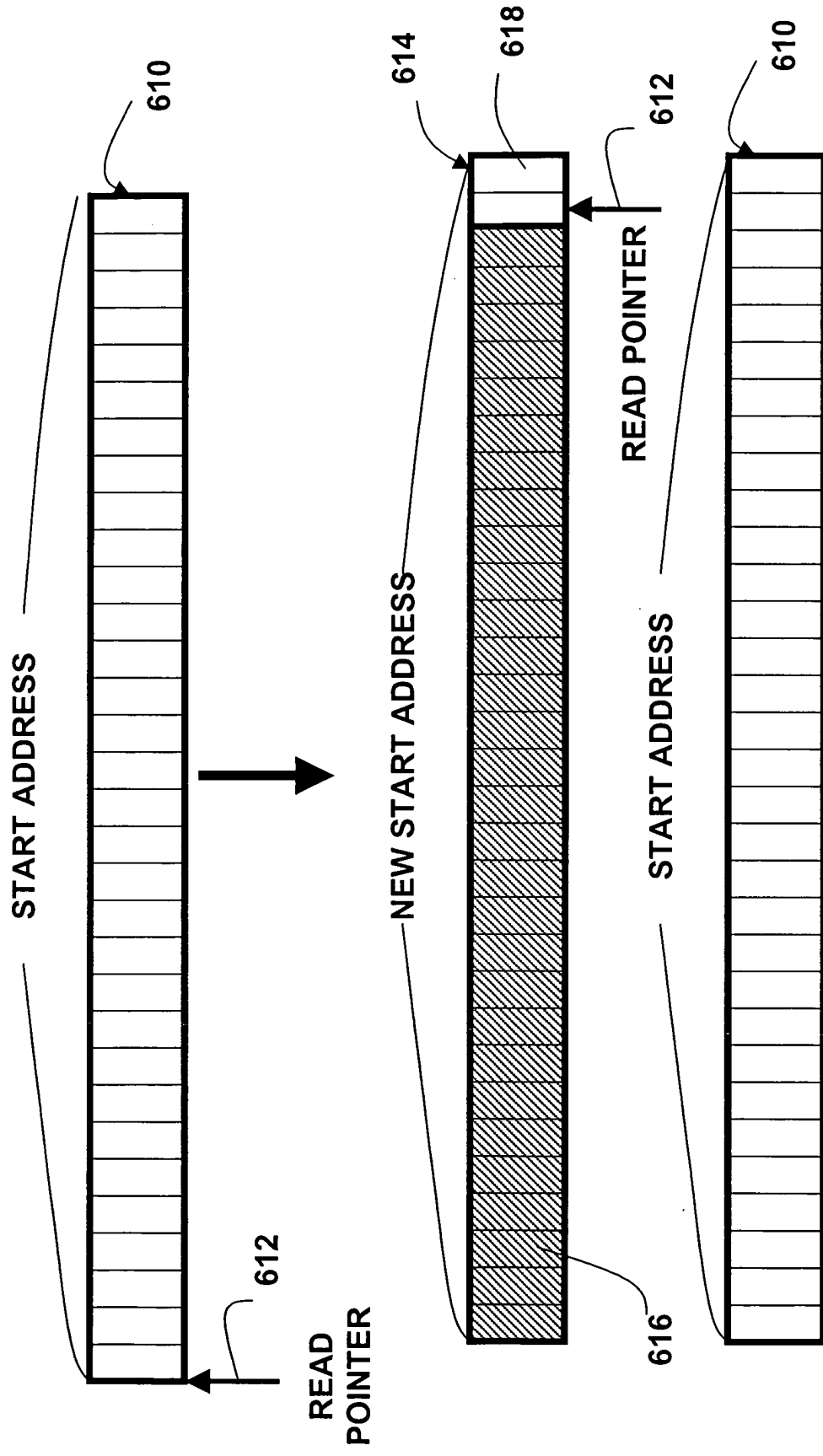
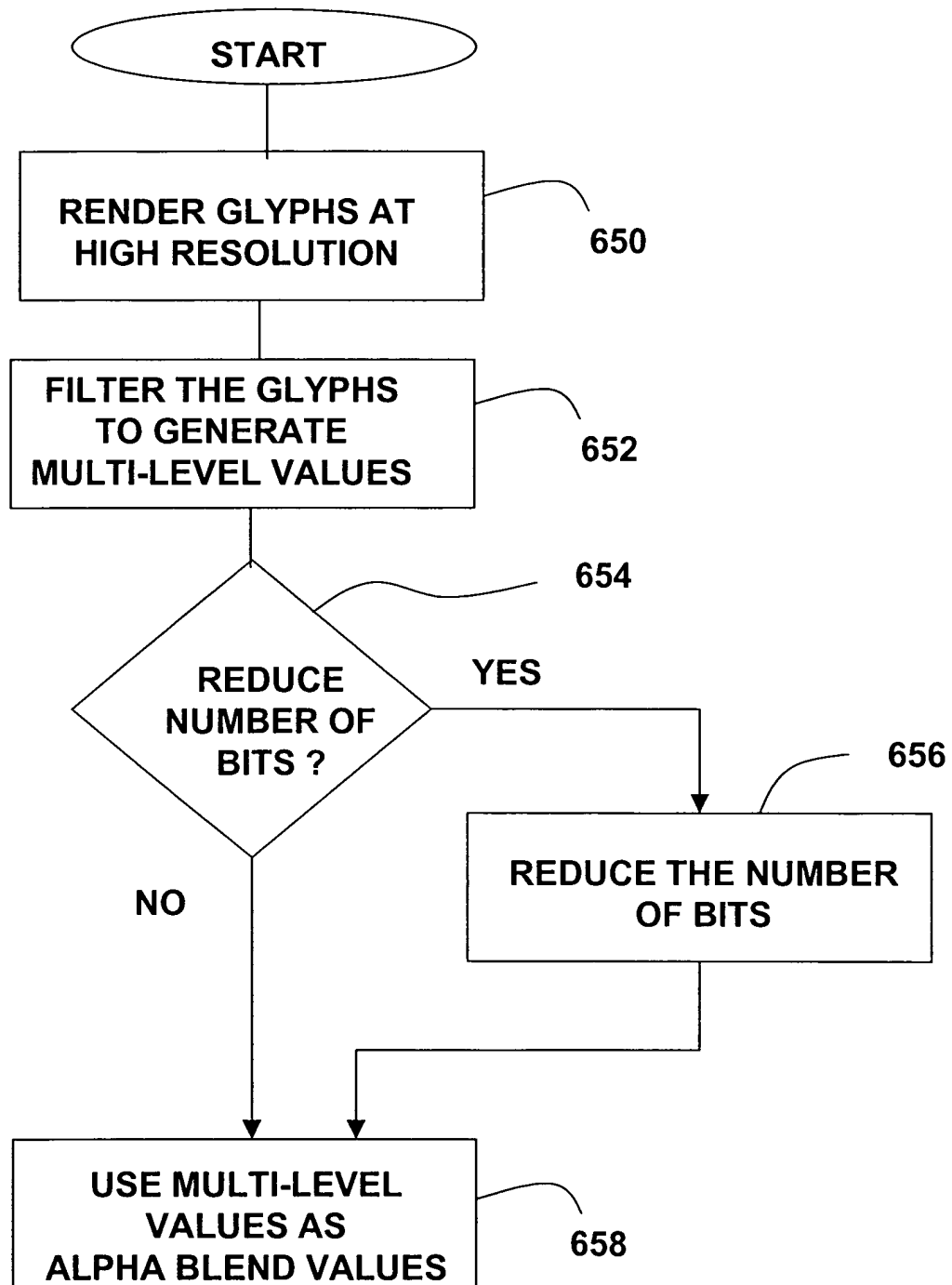


FIG. 16





**FIG. 17**

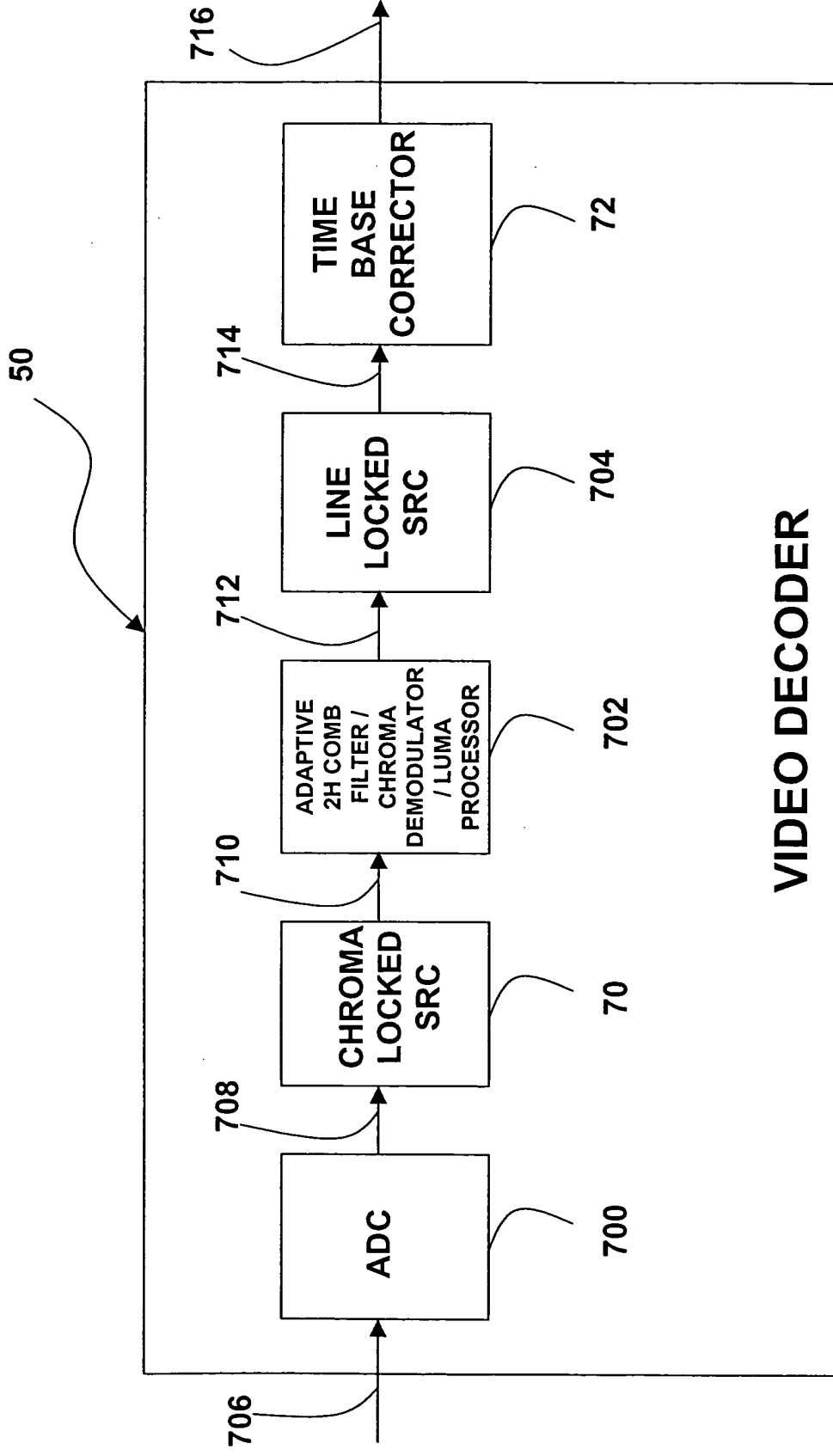


FIG. 18

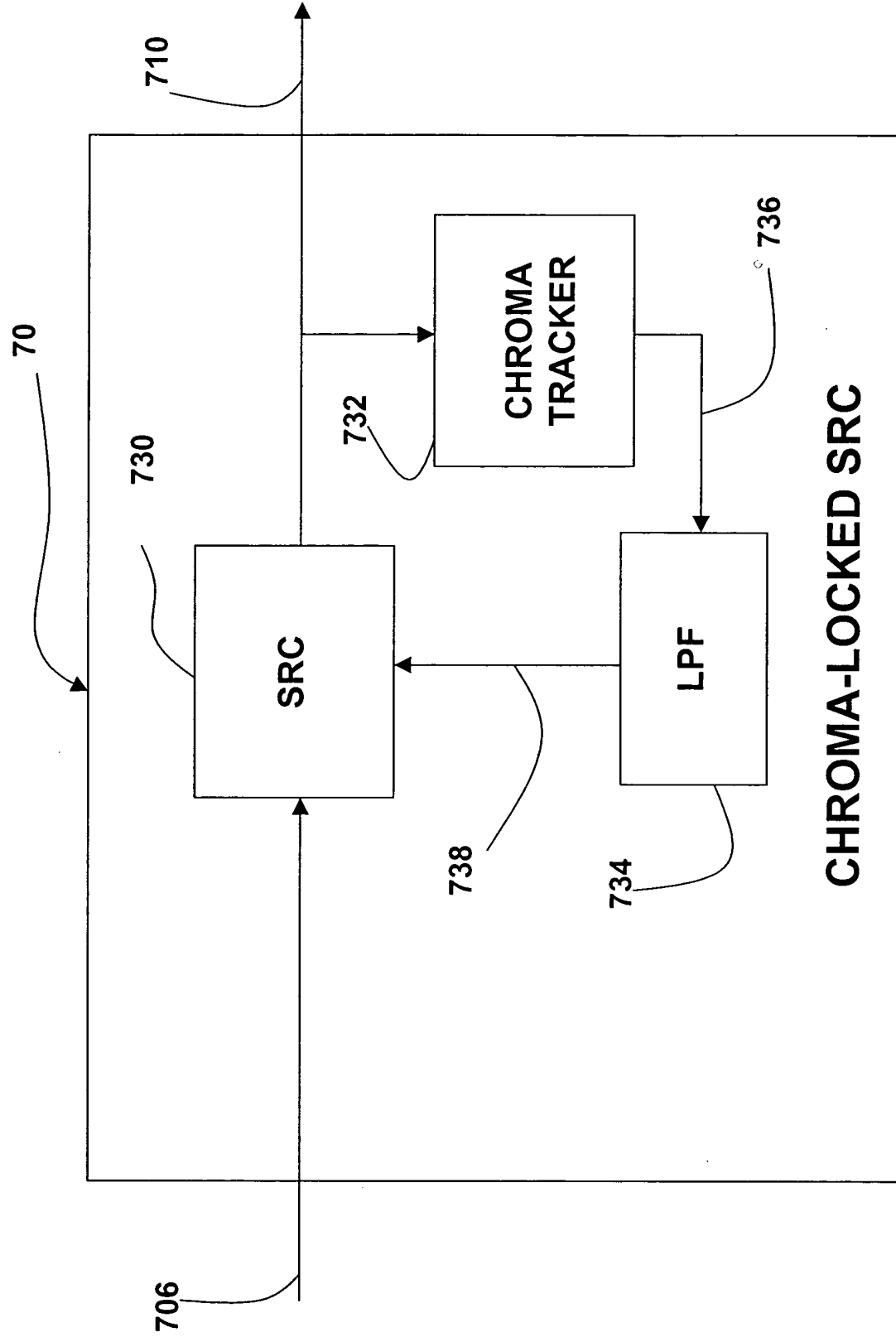


FIG. 19



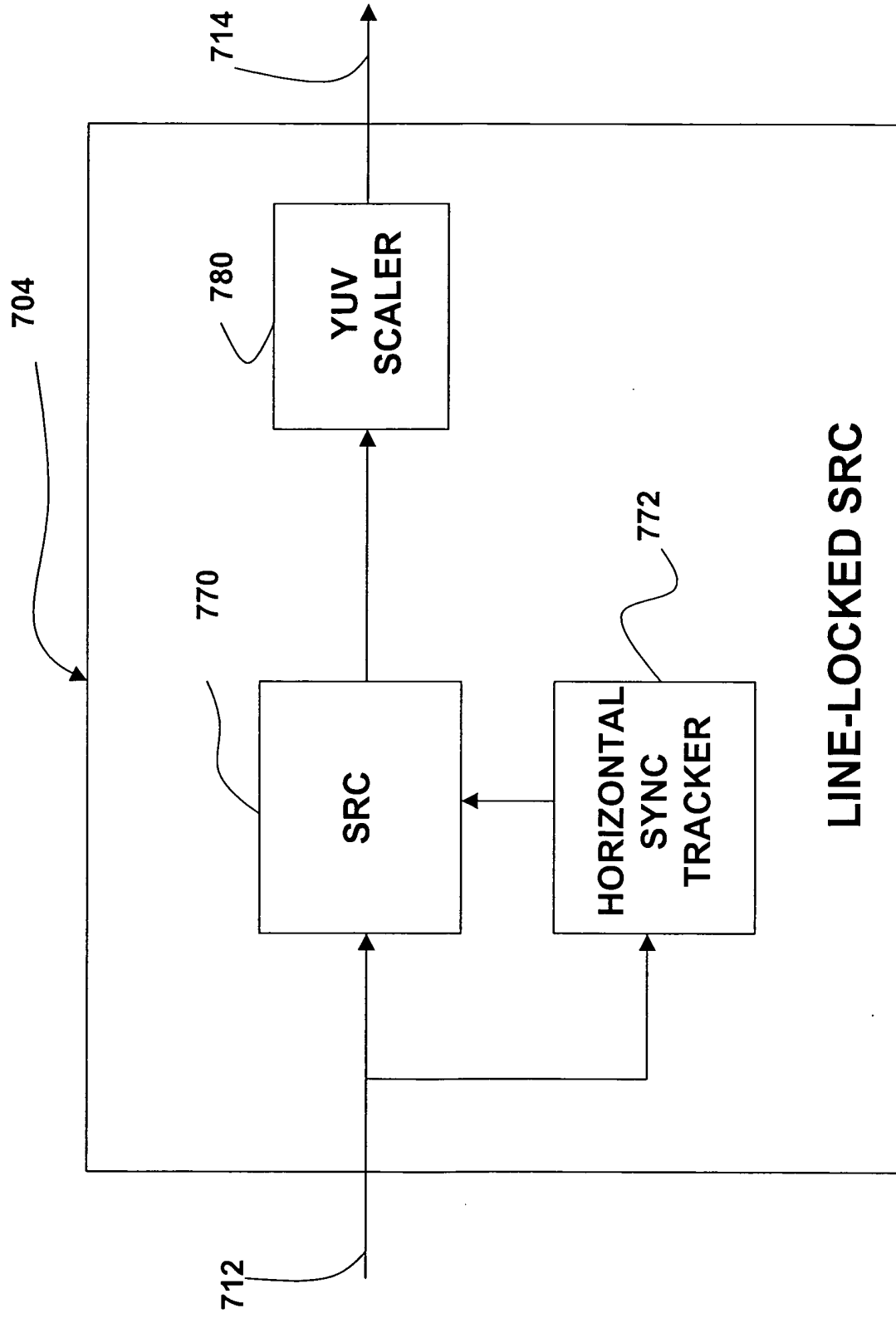


FIG. 21

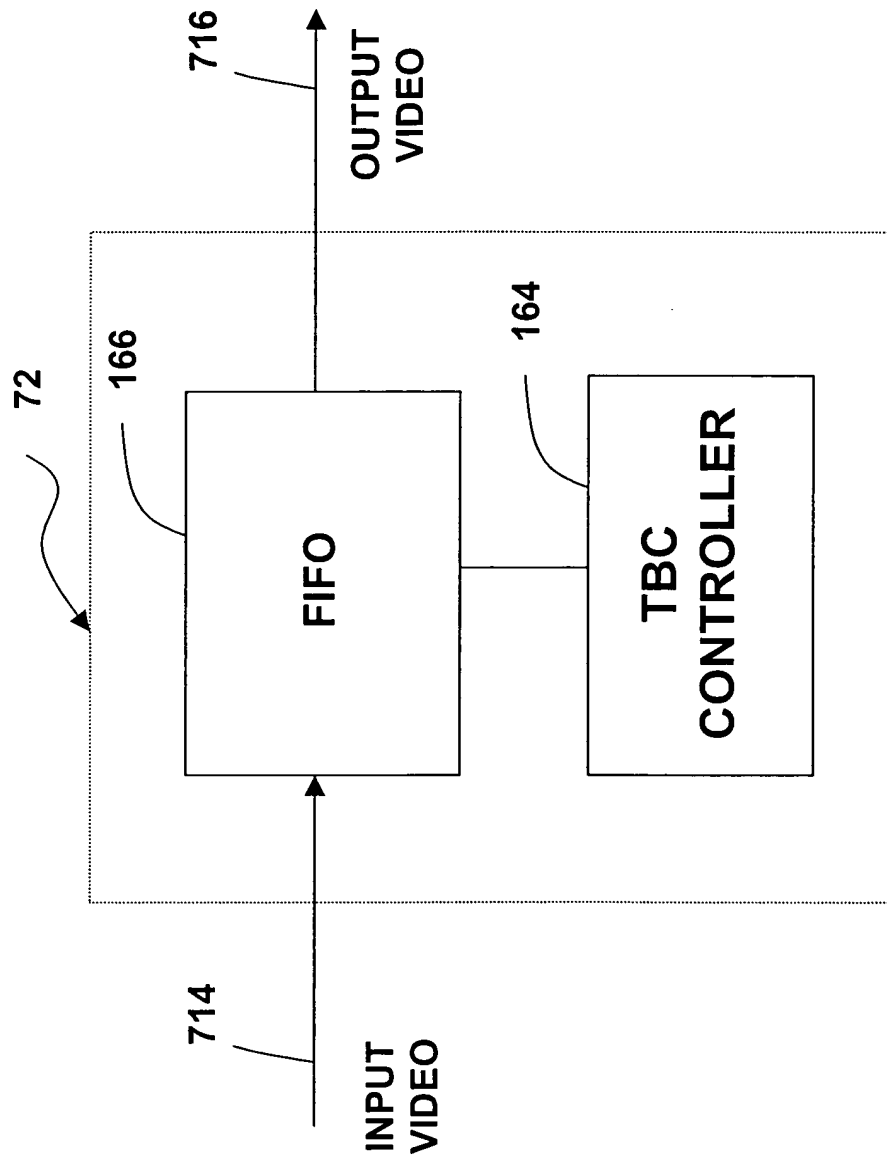
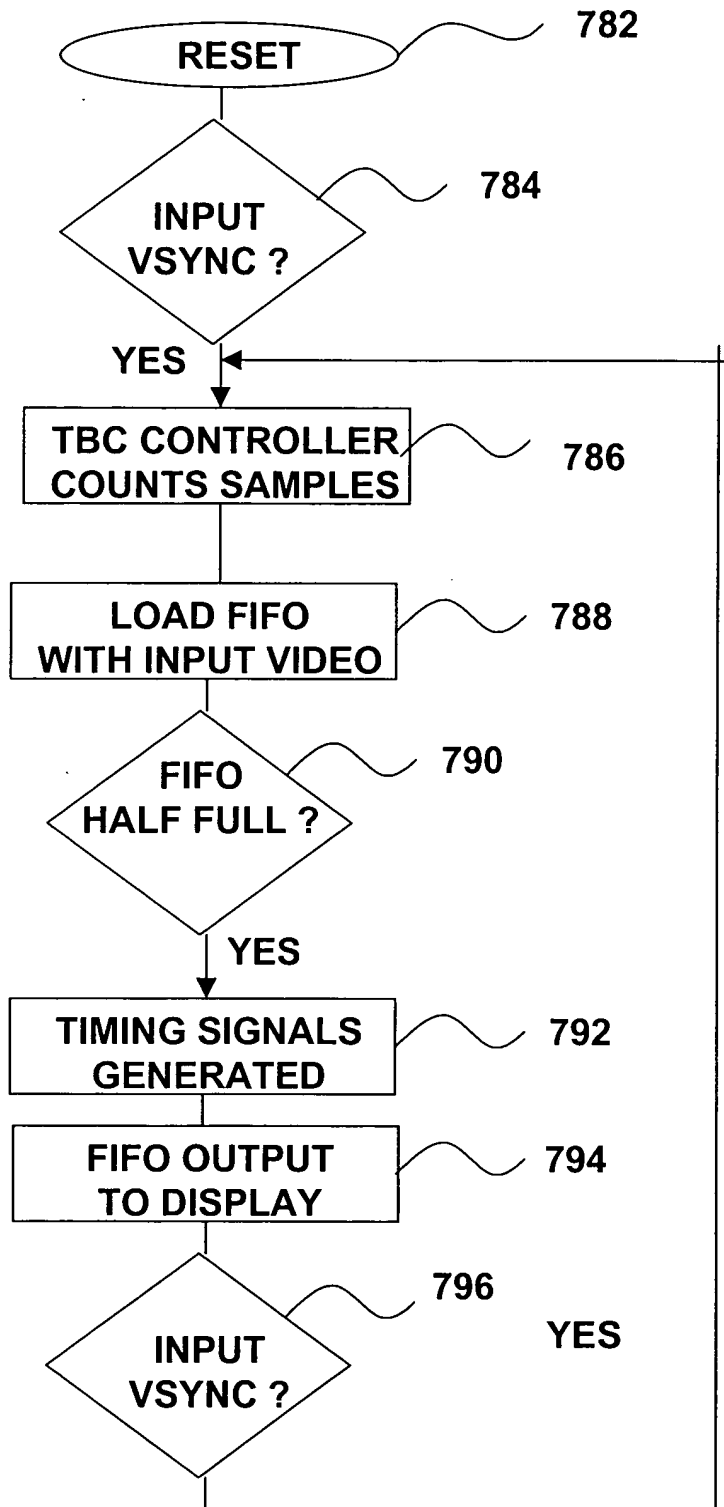


FIG. 22



**FIG. 23**





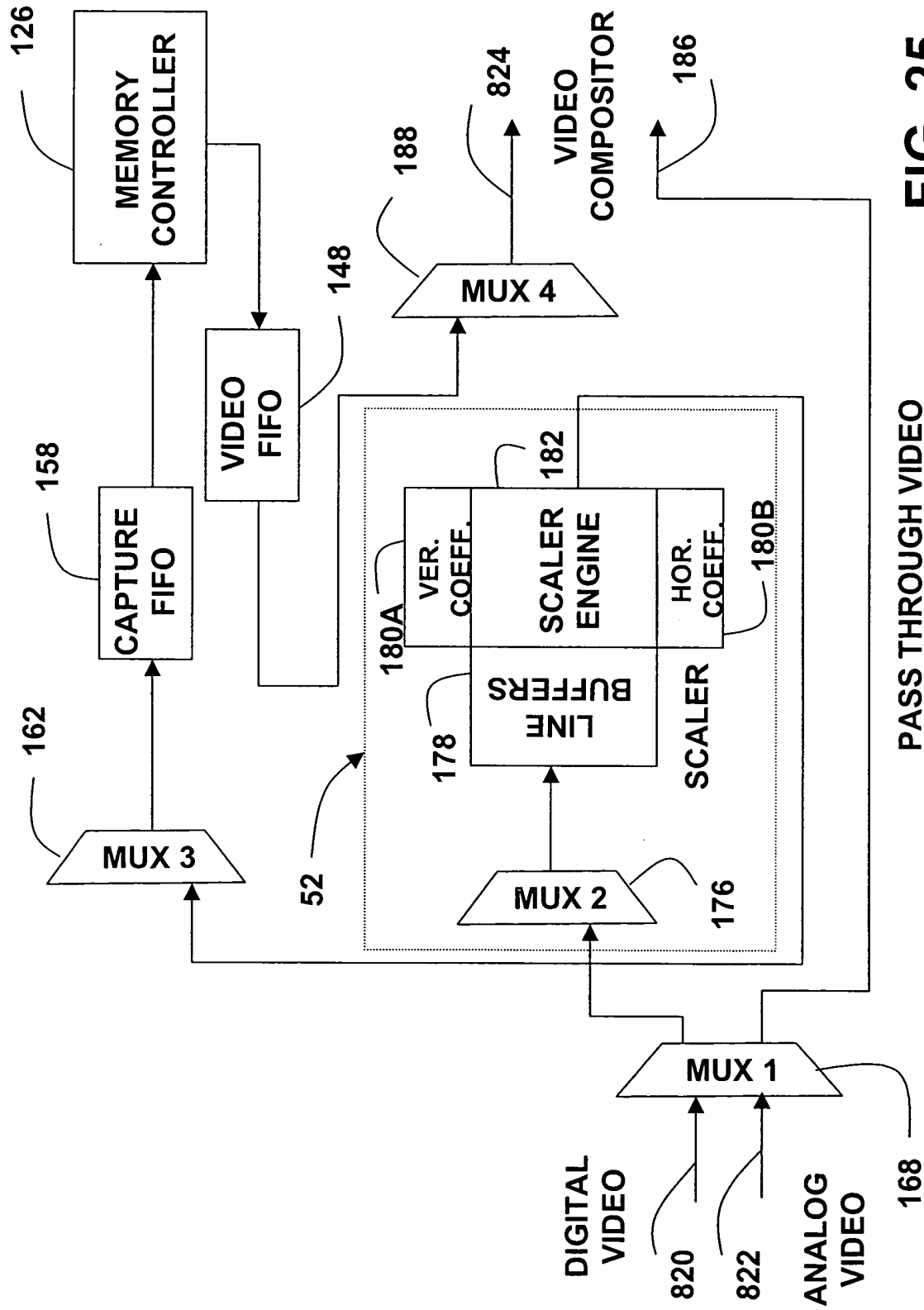


FIG. 25

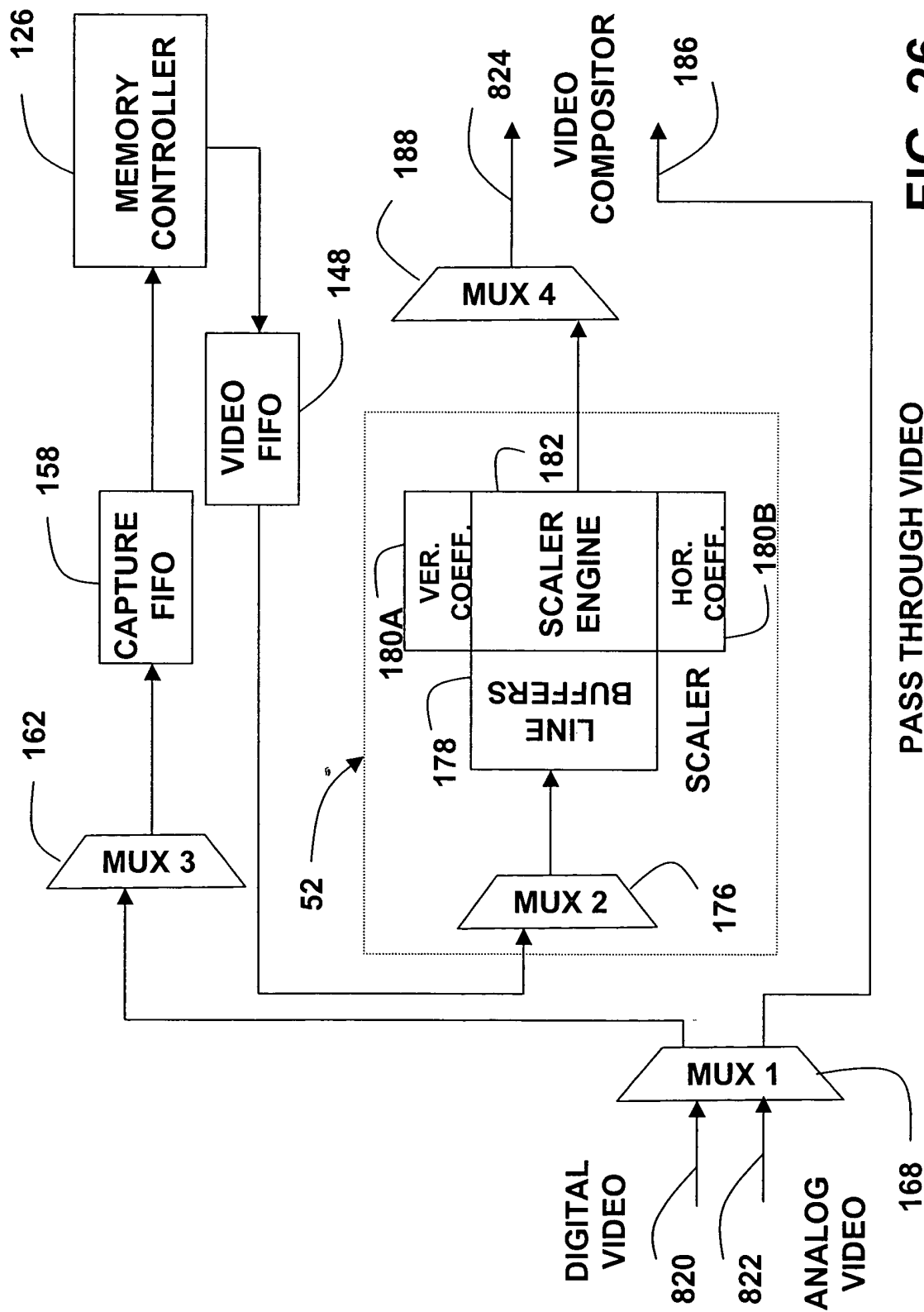


FIG. 26

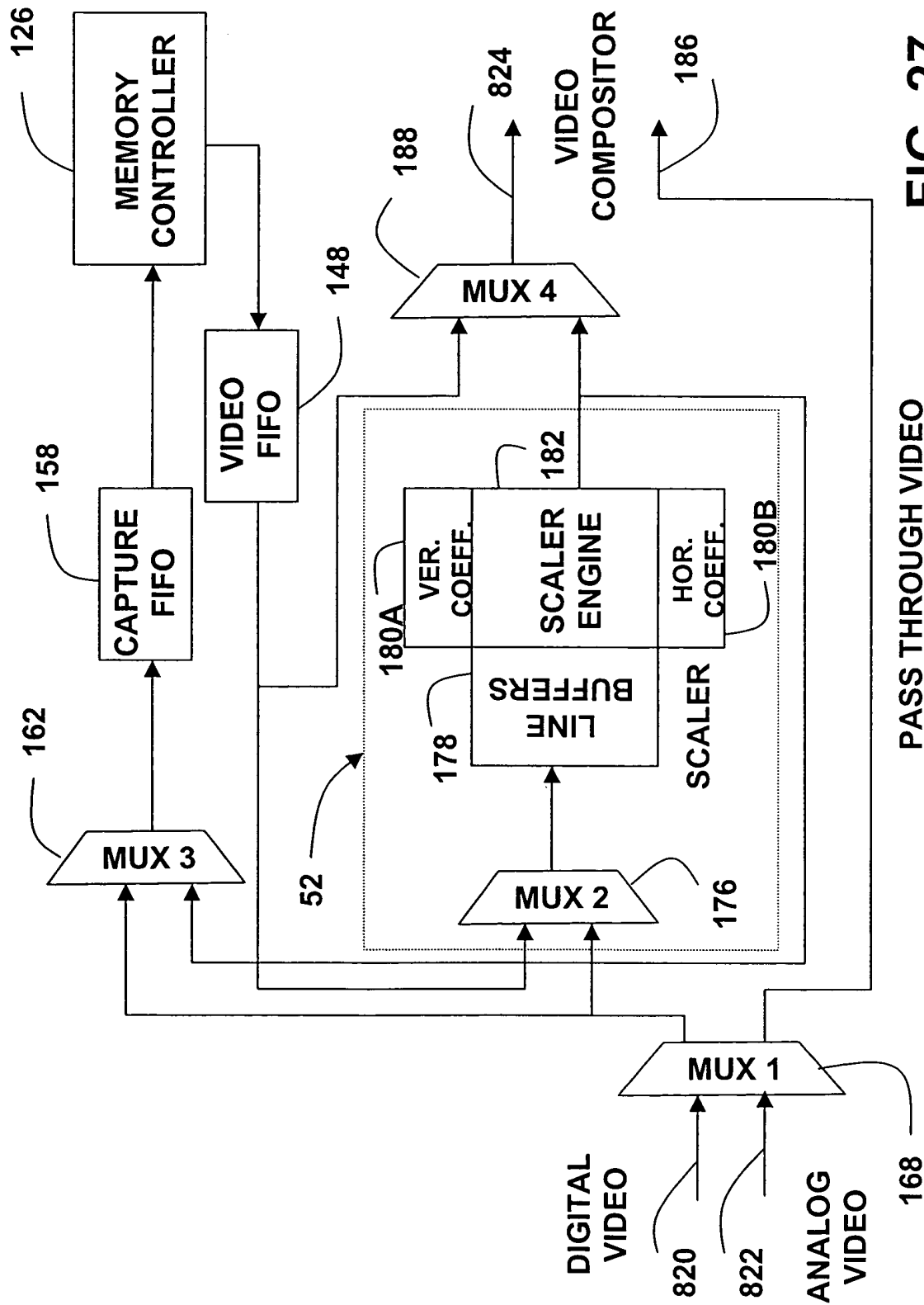
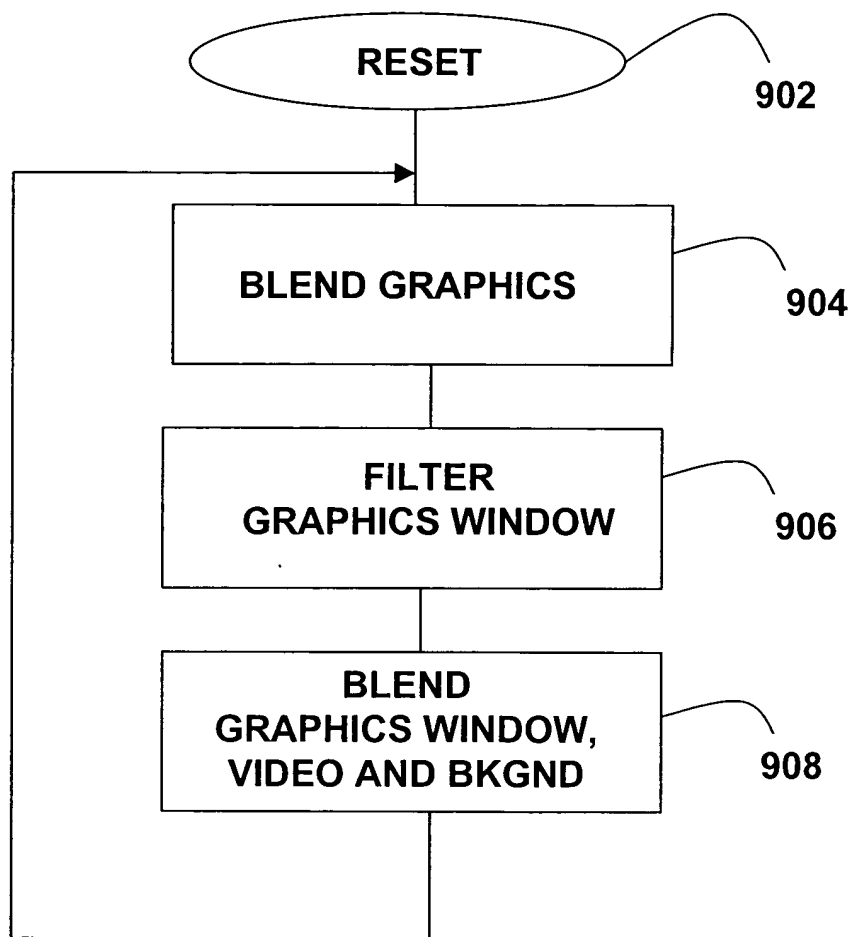
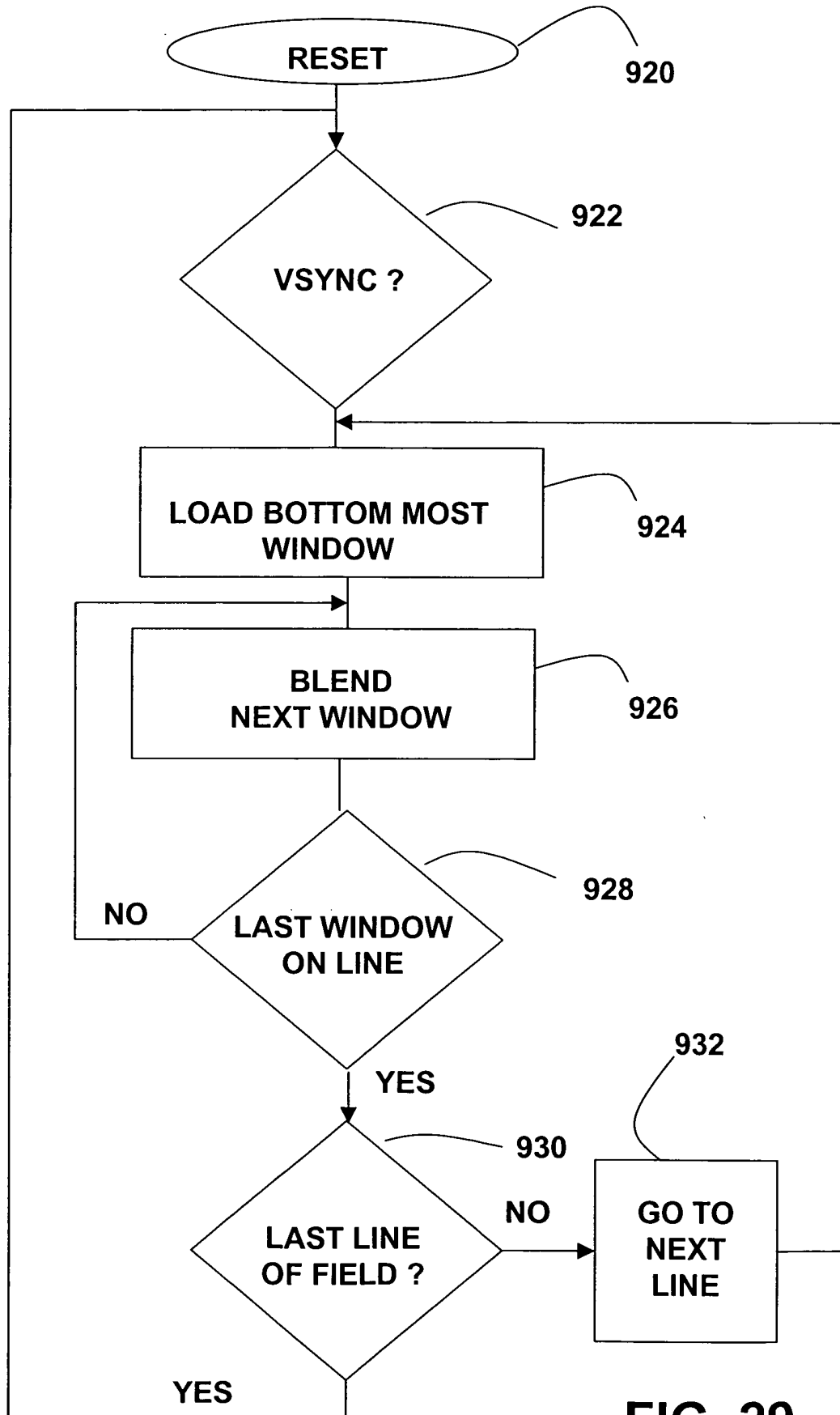


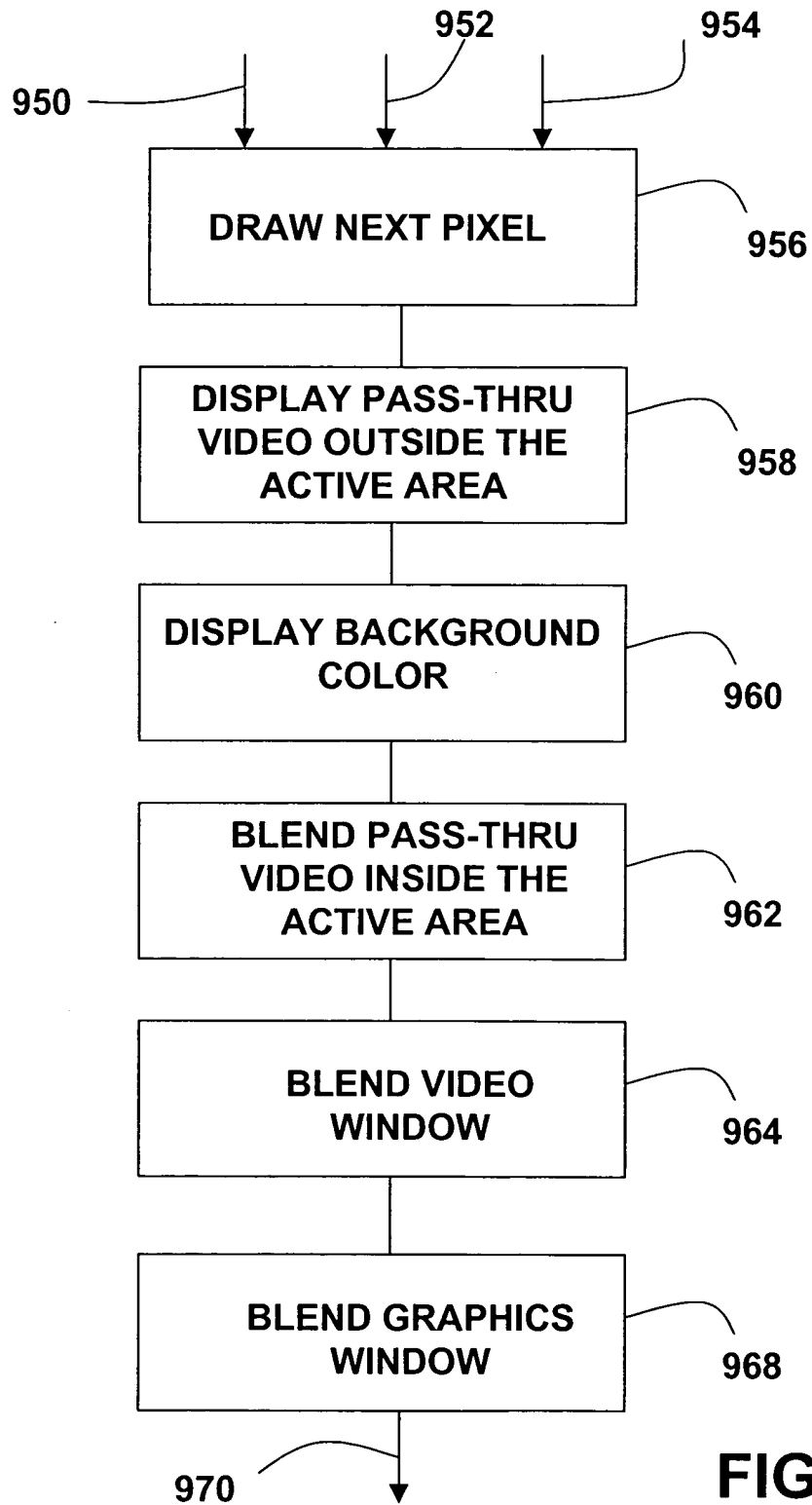
FIG. 27



**FIG. 28**



**FIG. 29**



**FIG. 30**

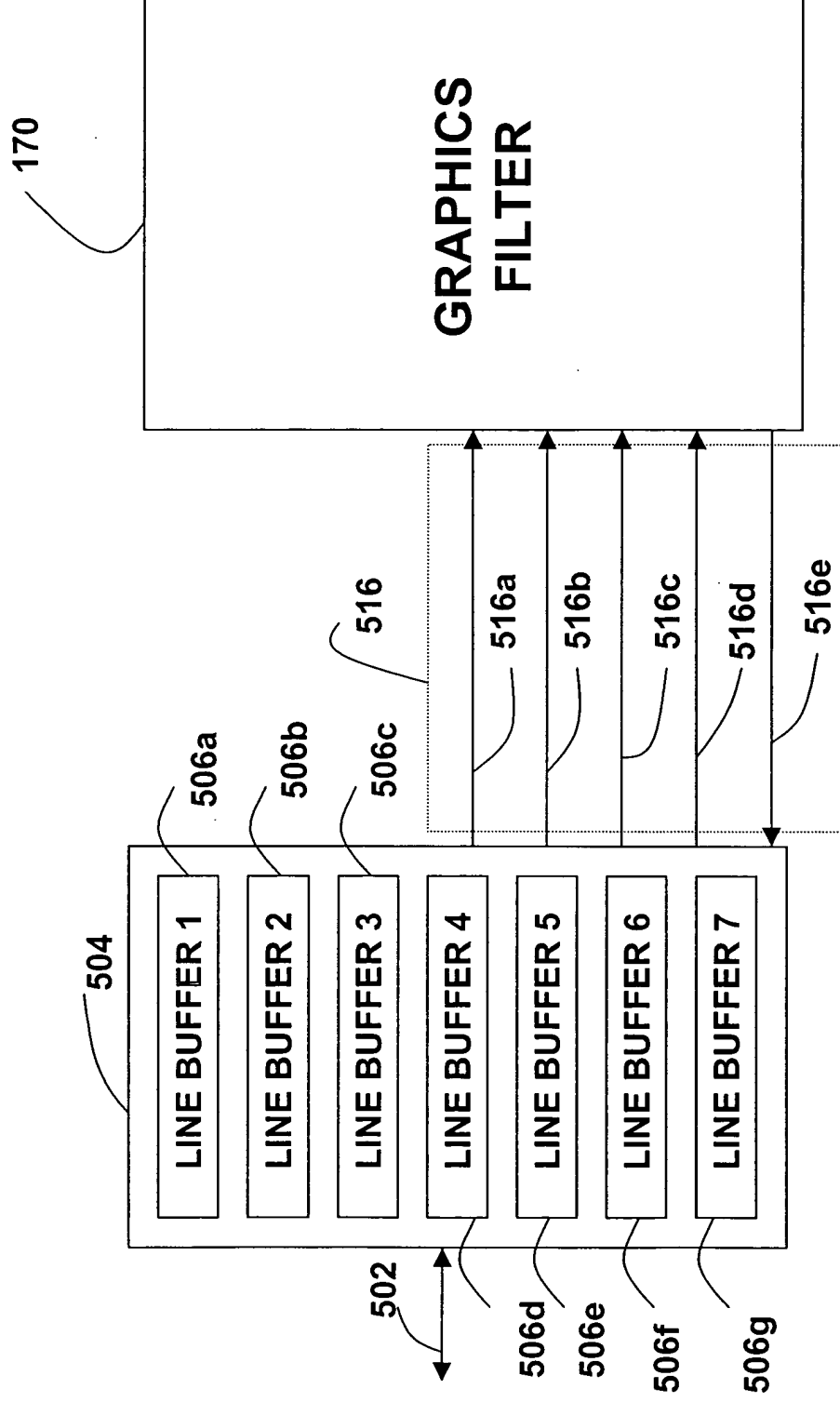


FIG. 31

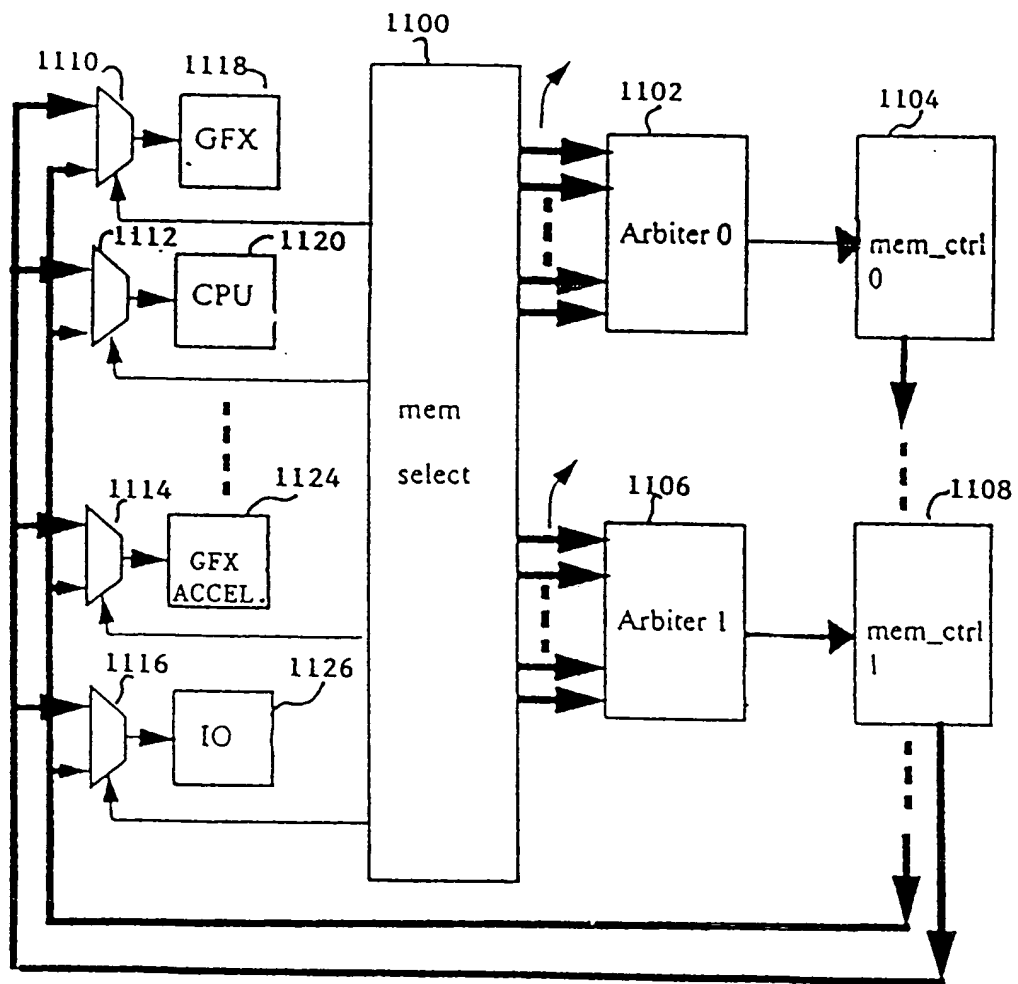


FIG. 32



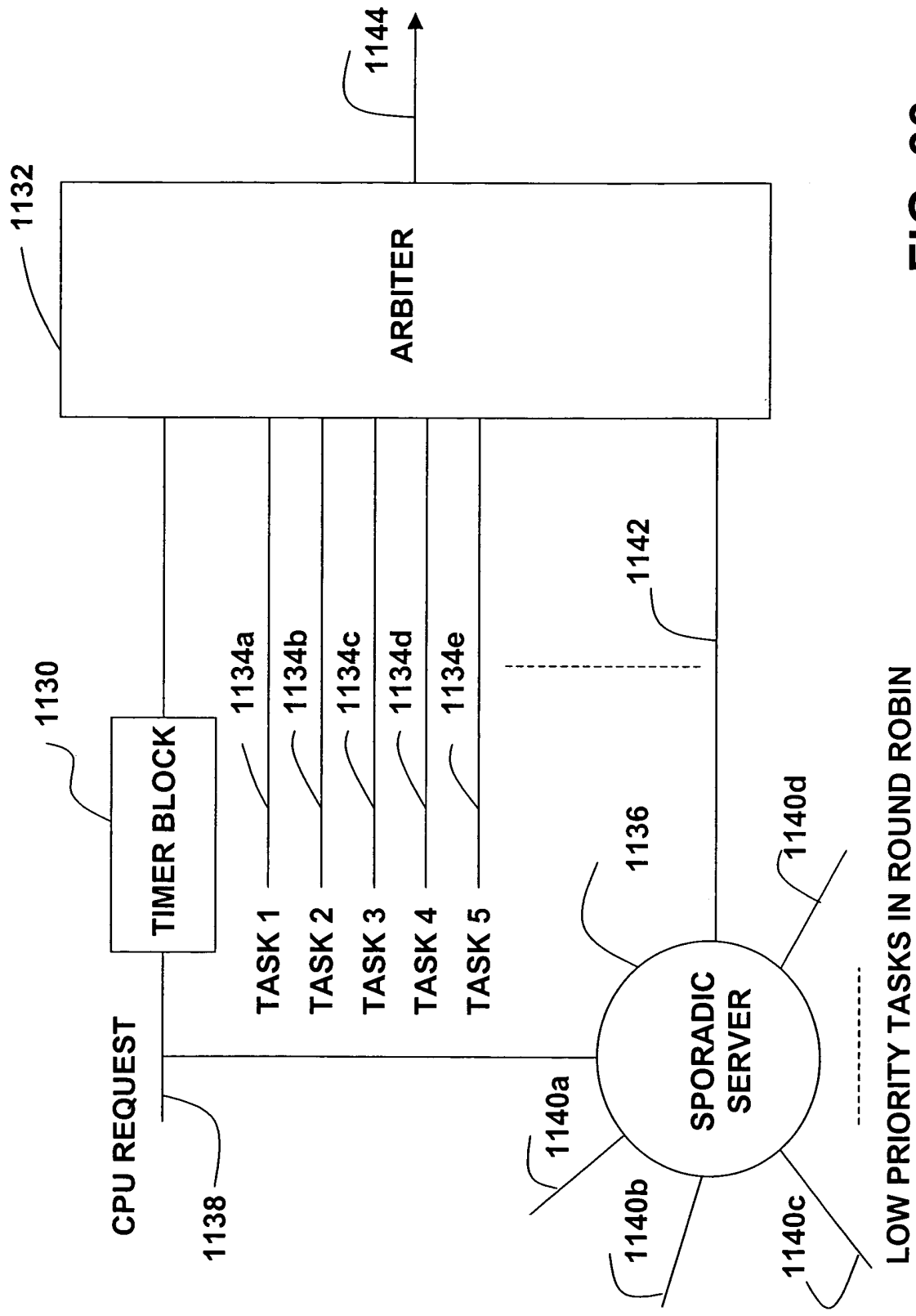


FIG. 33

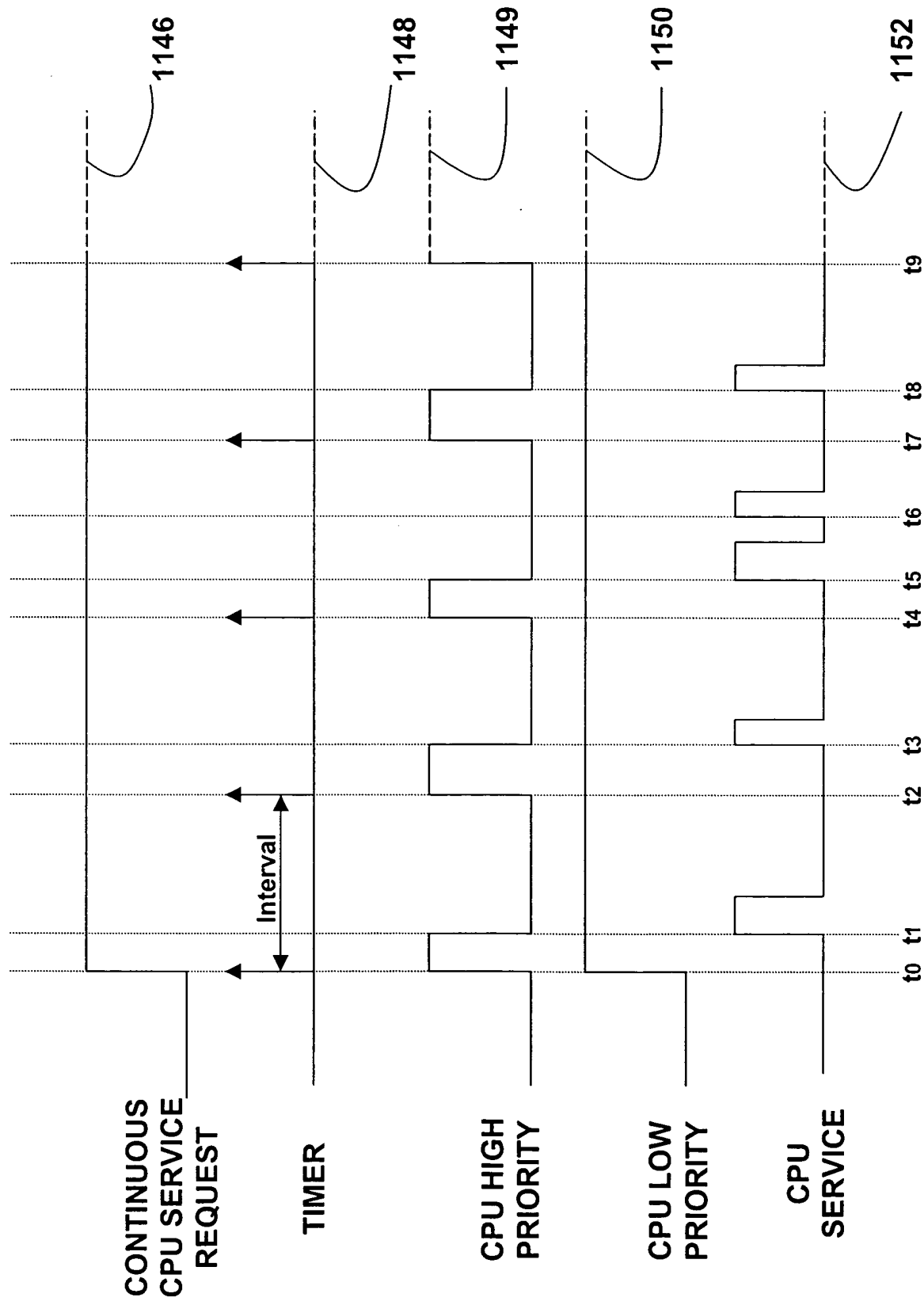


FIG. 34

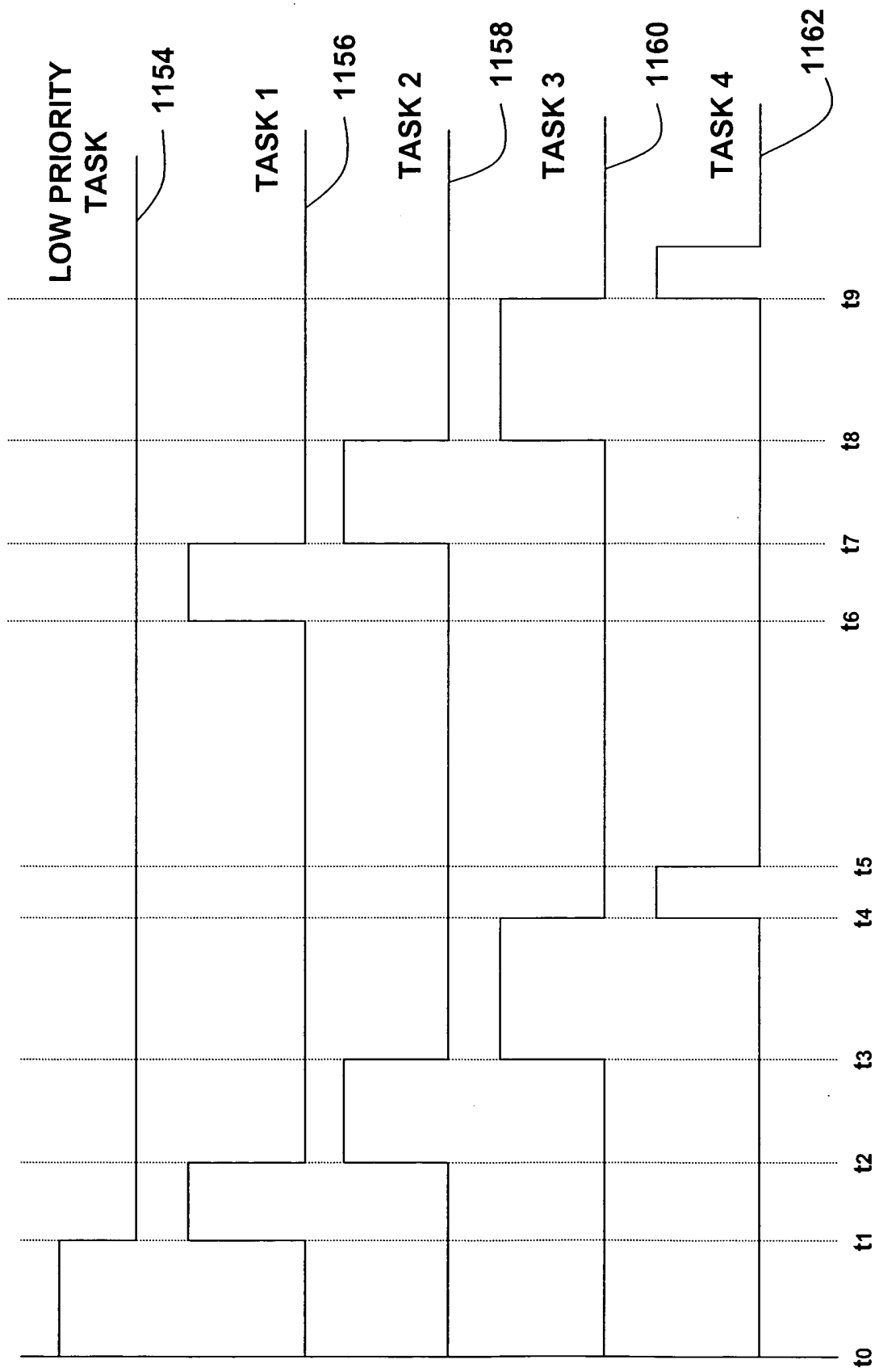


FIG. 35

Highest Priority

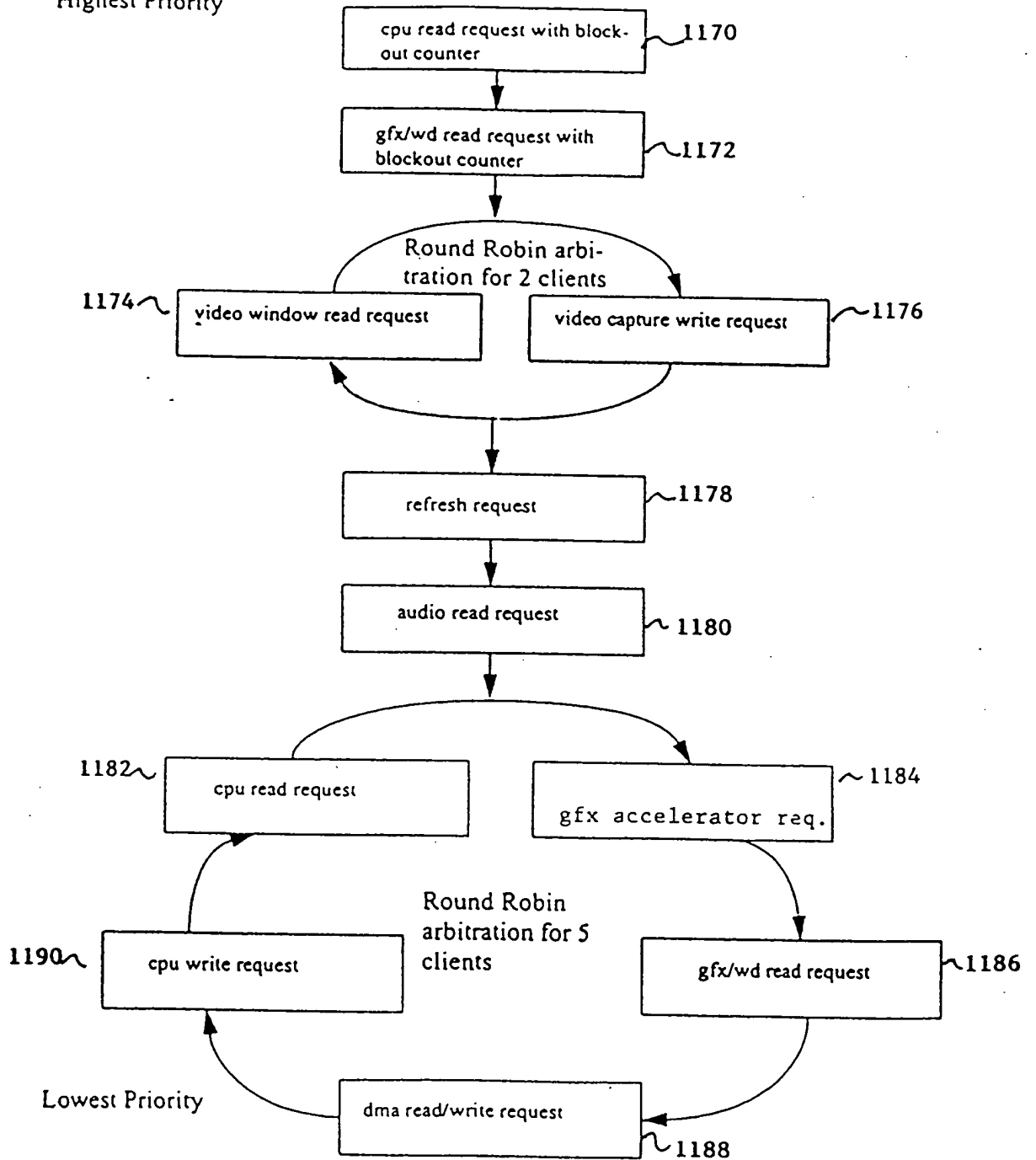


FIG. 36

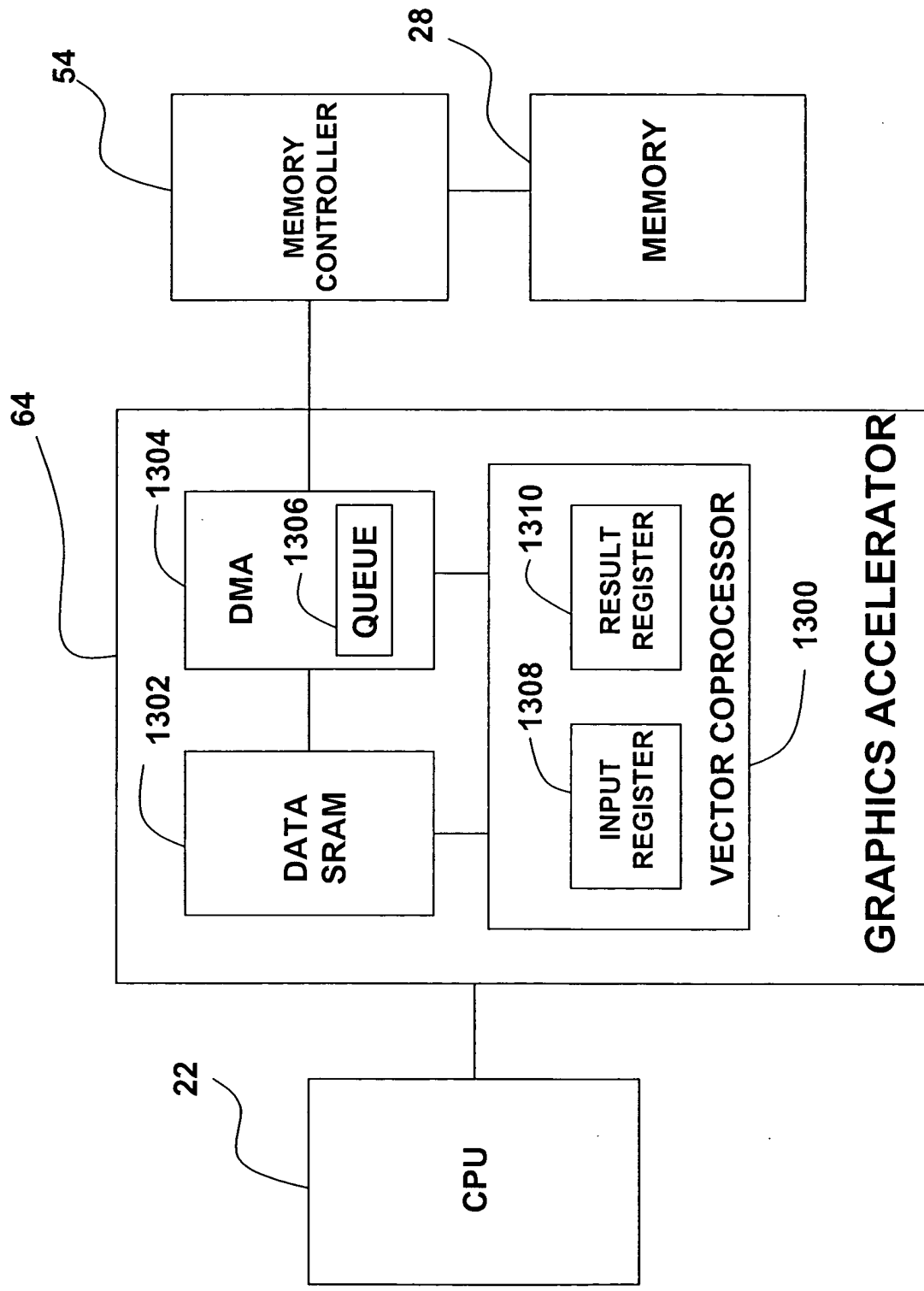


FIG. 37

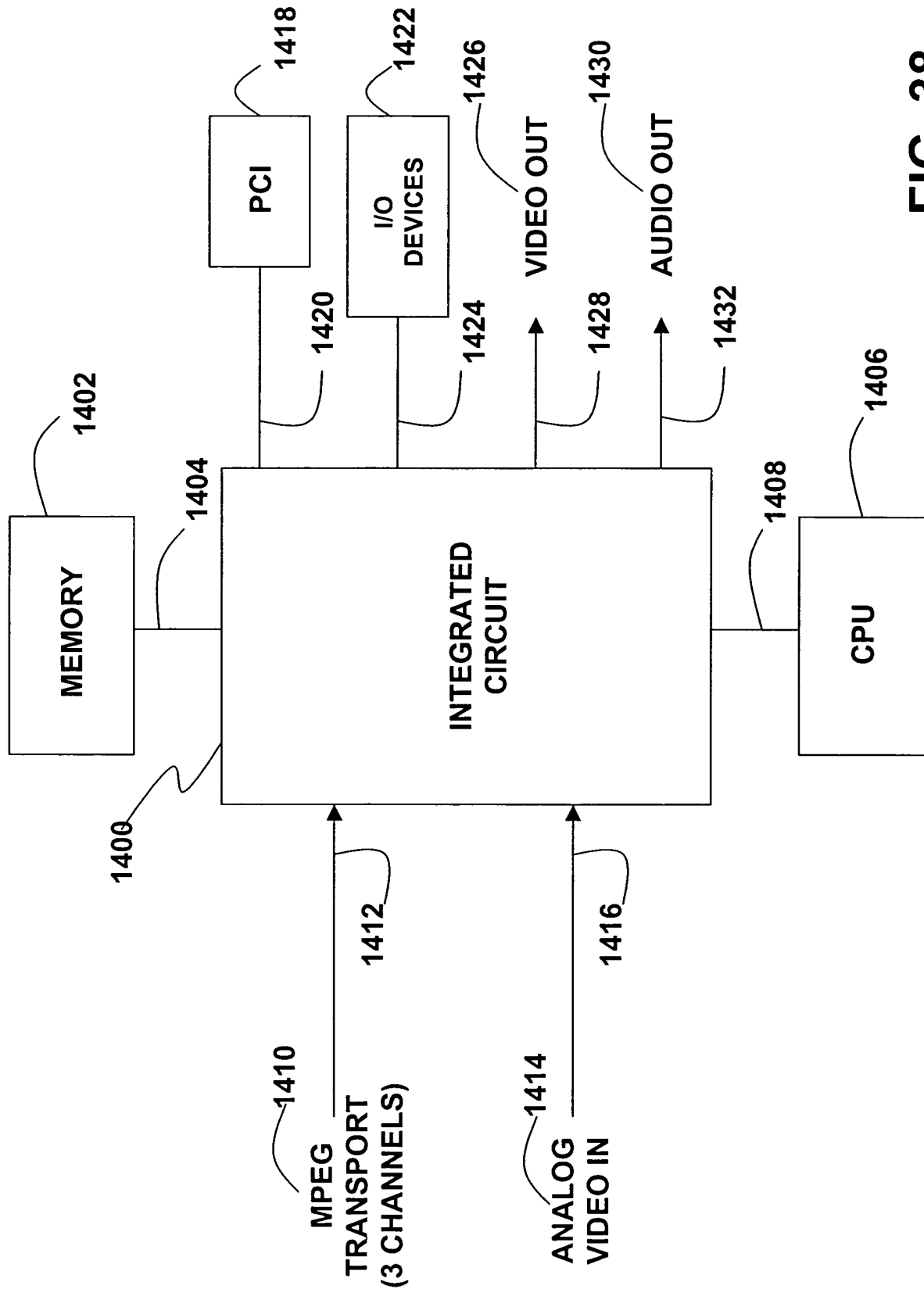


FIG. 38

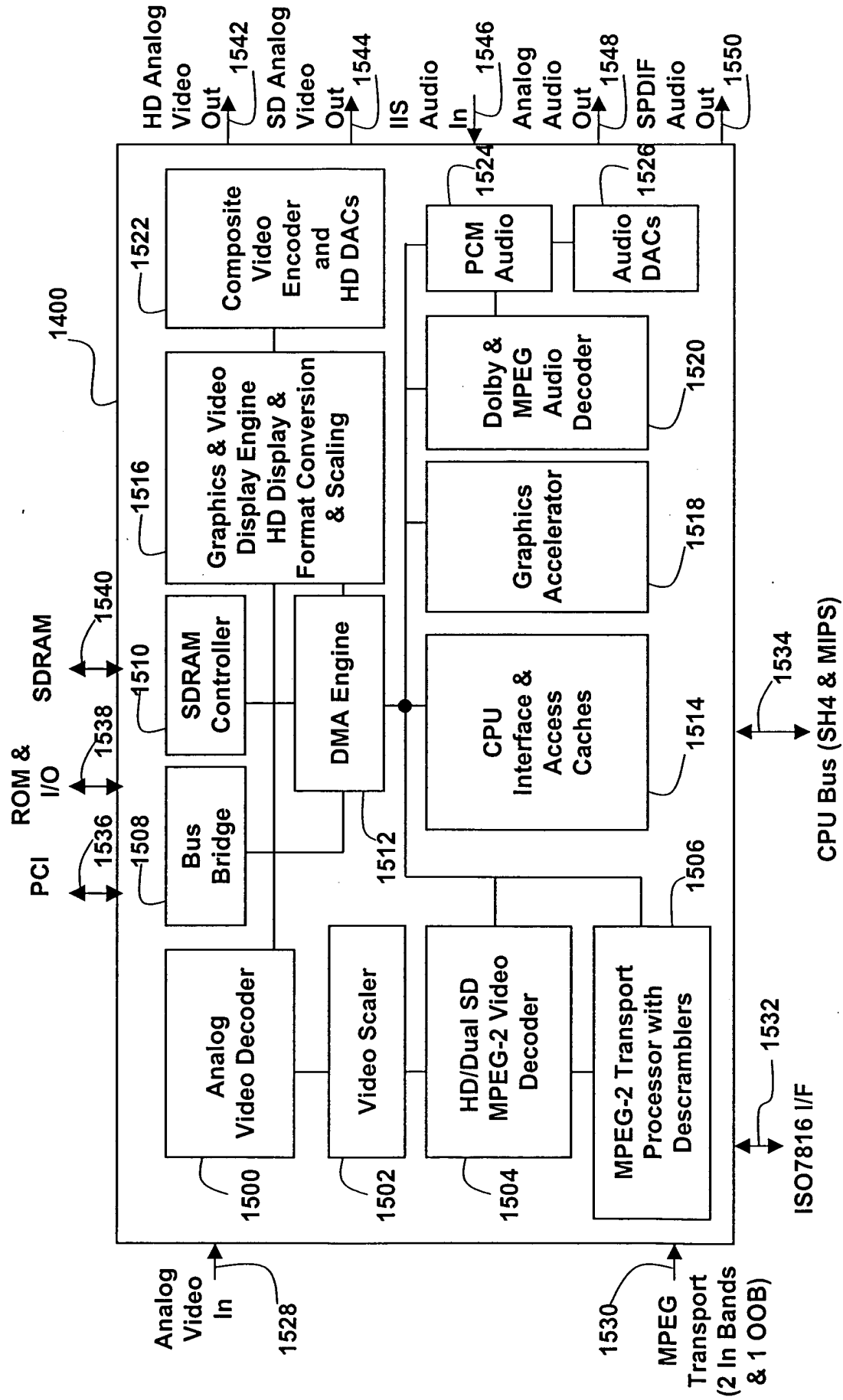


FIG. 39





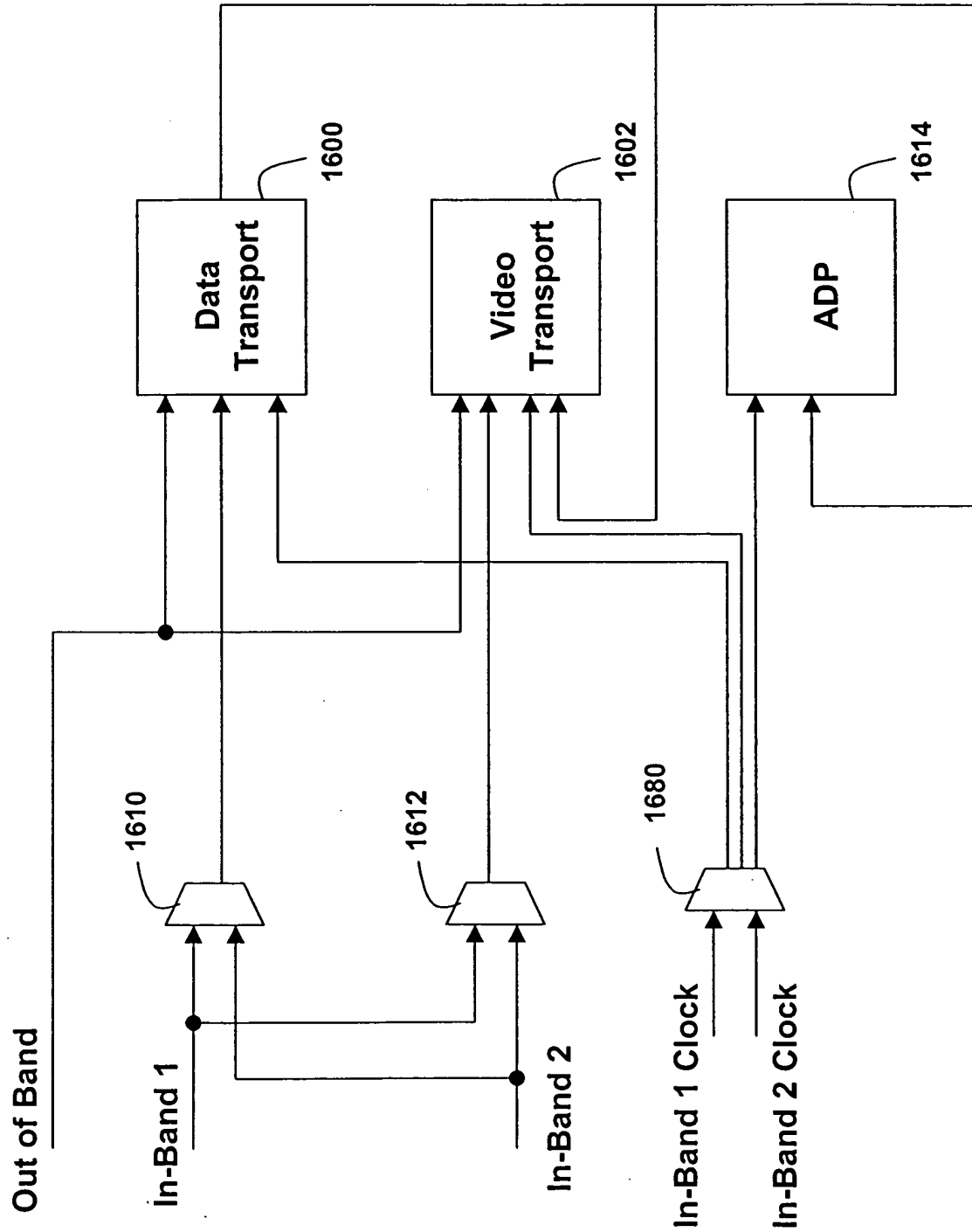


FIG. 41

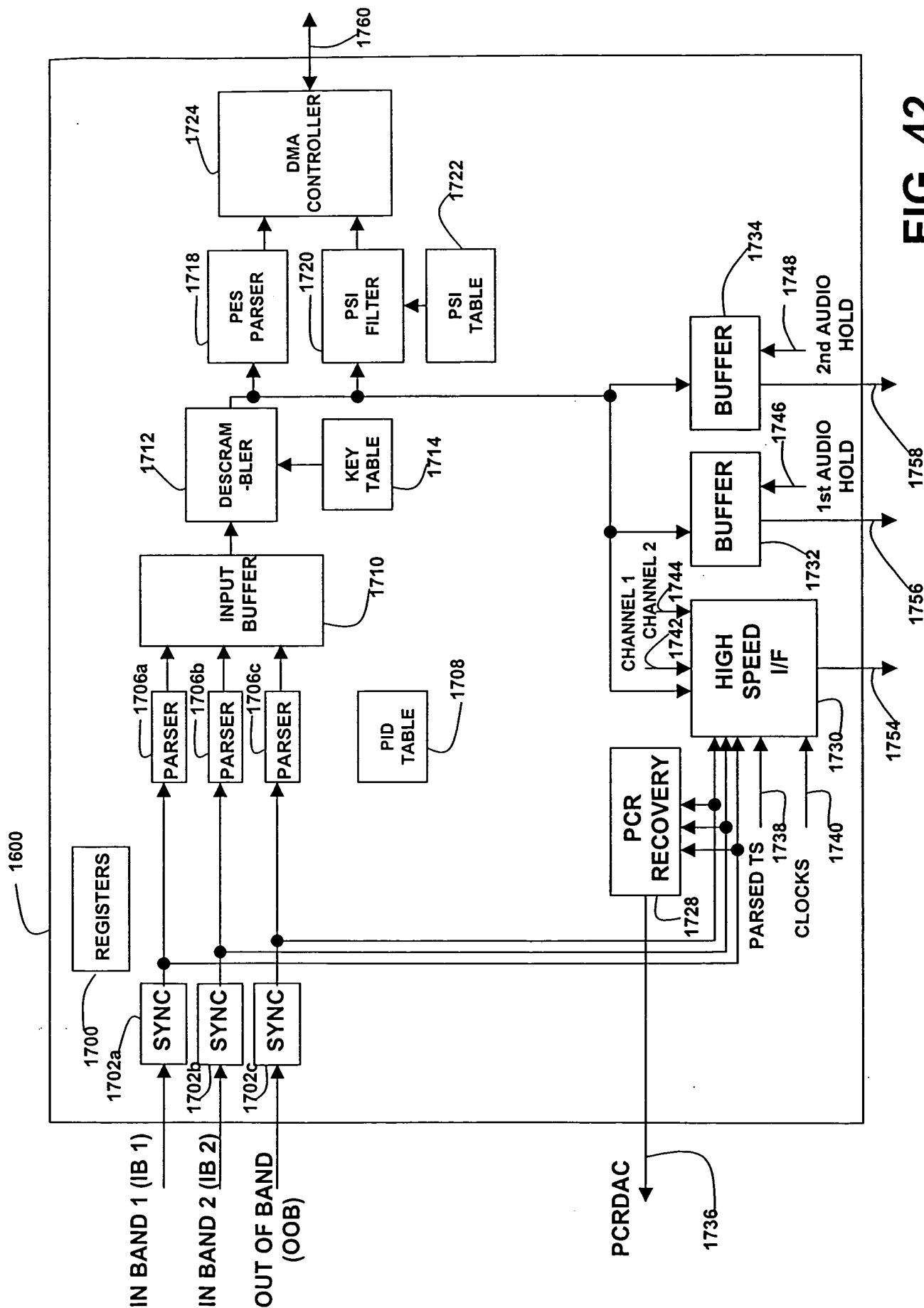


FIG. 42

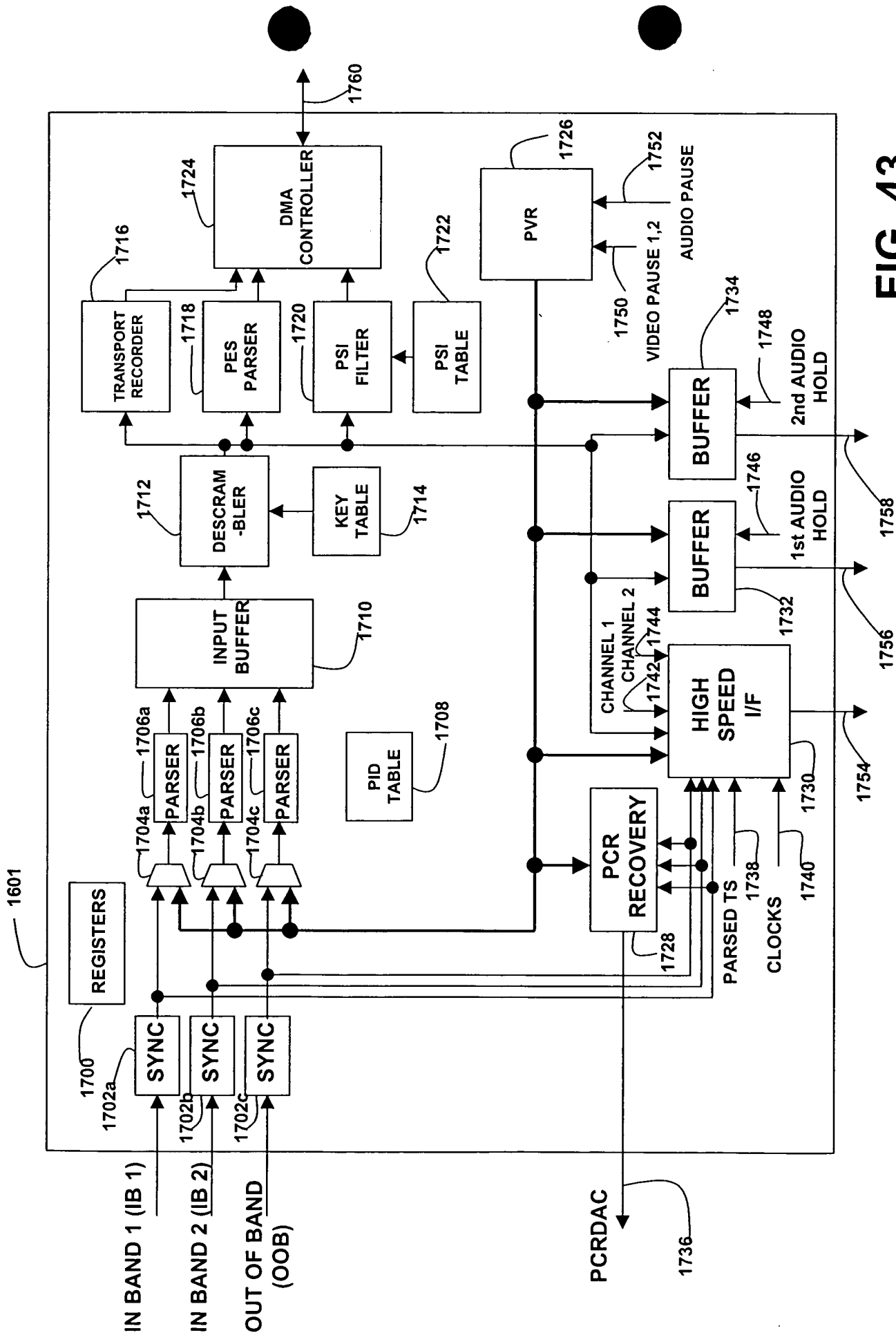


FIG. 43

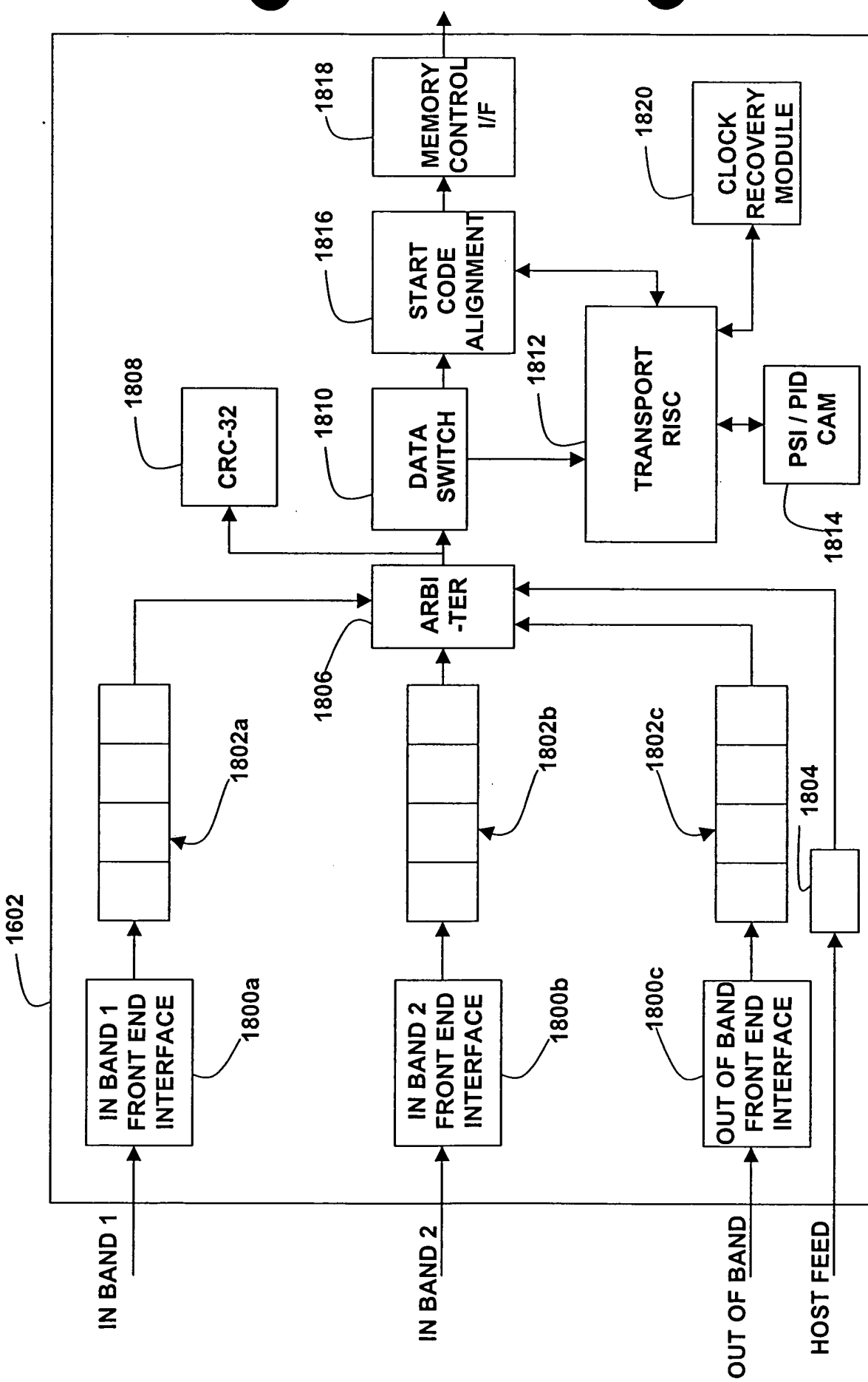


FIG. 44

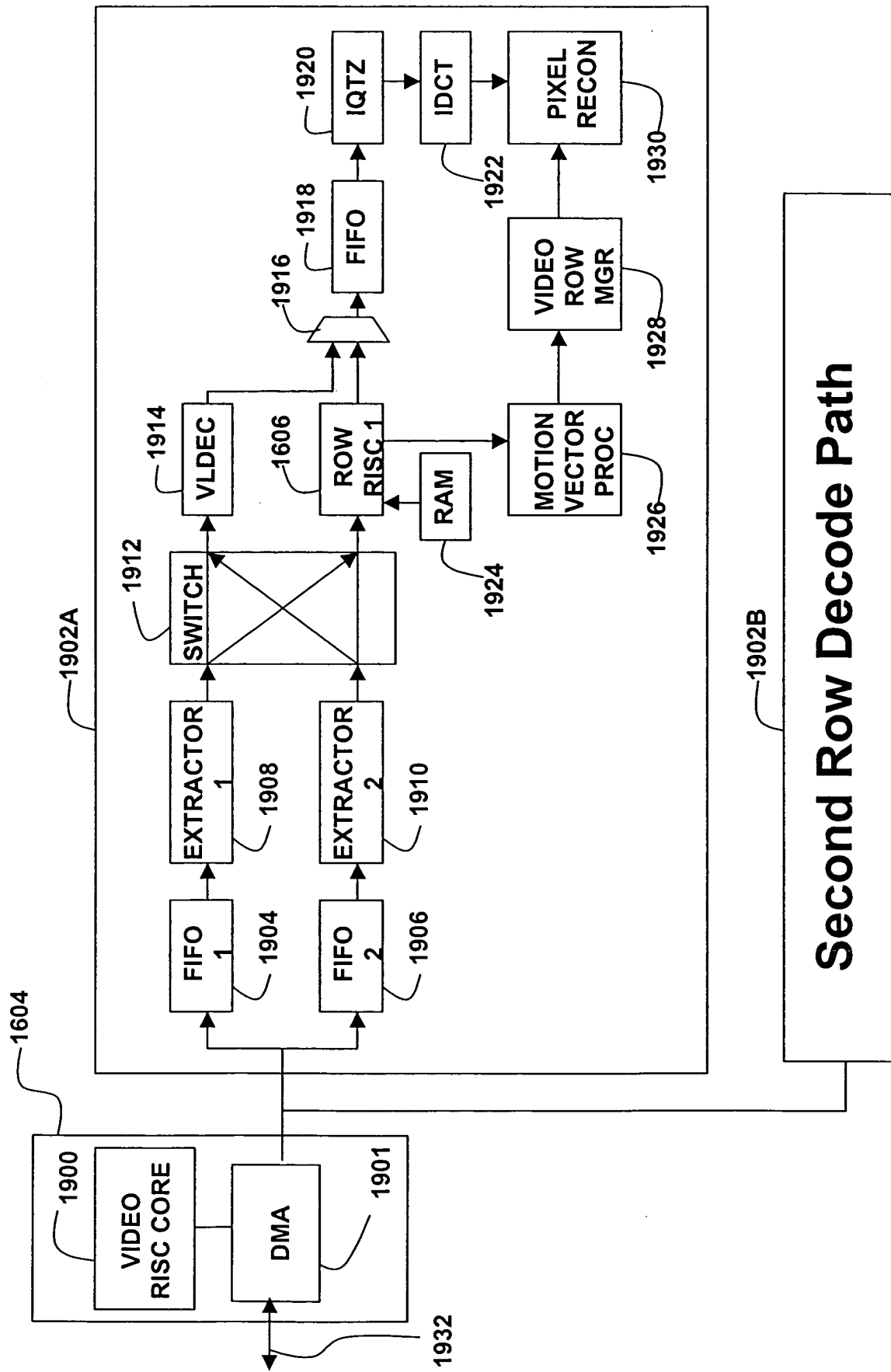


FIG. 45

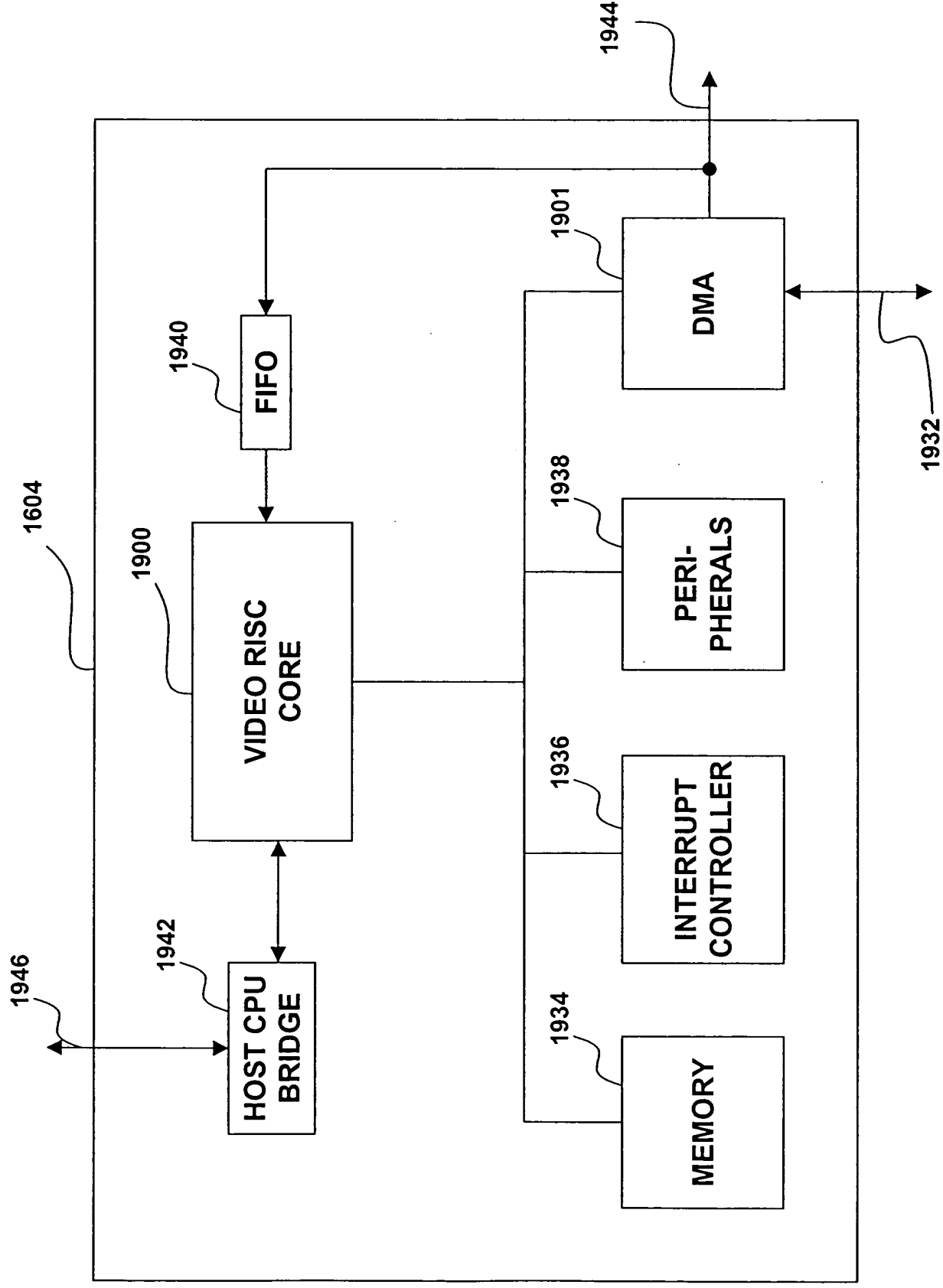


FIG. 46

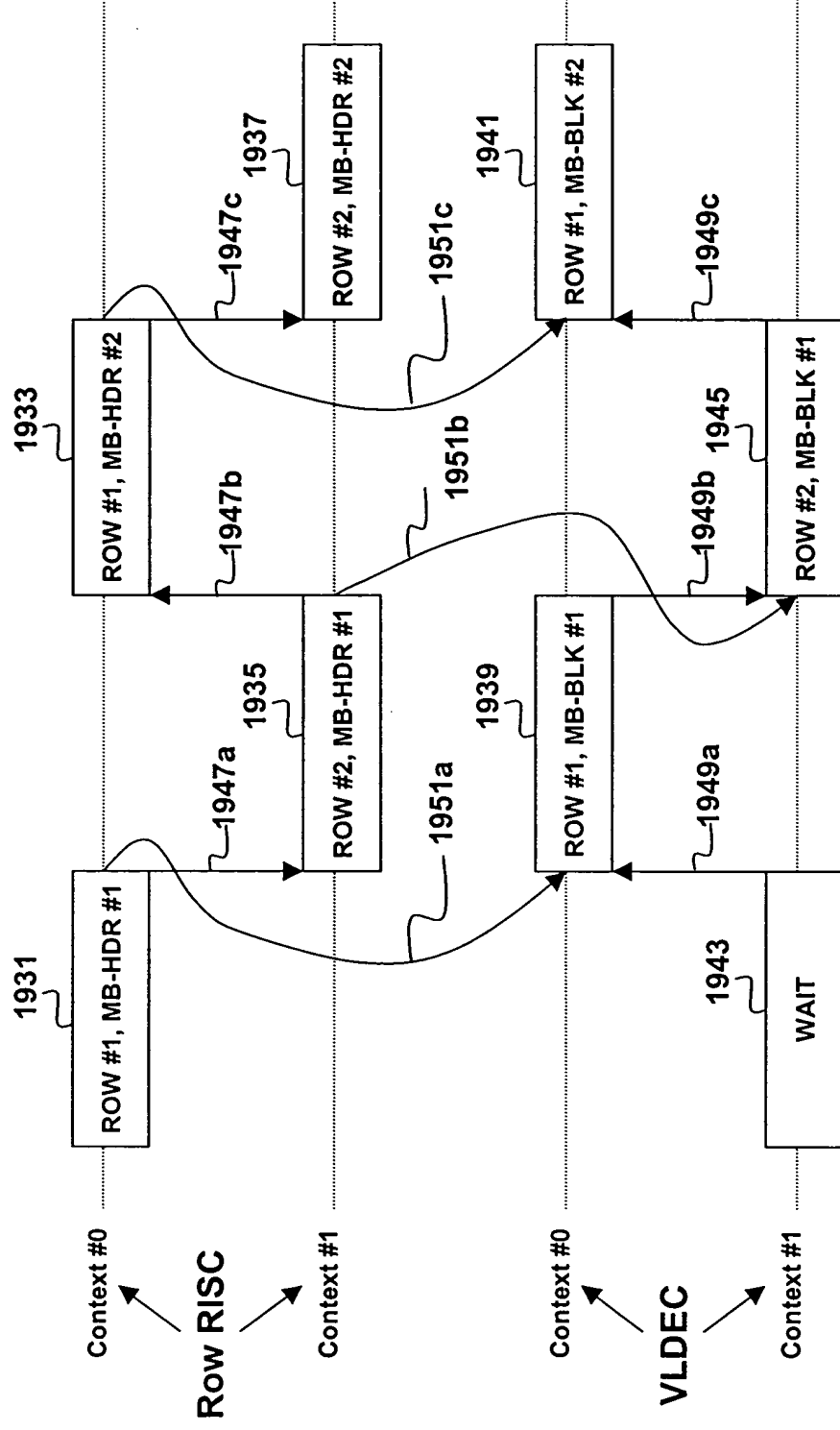
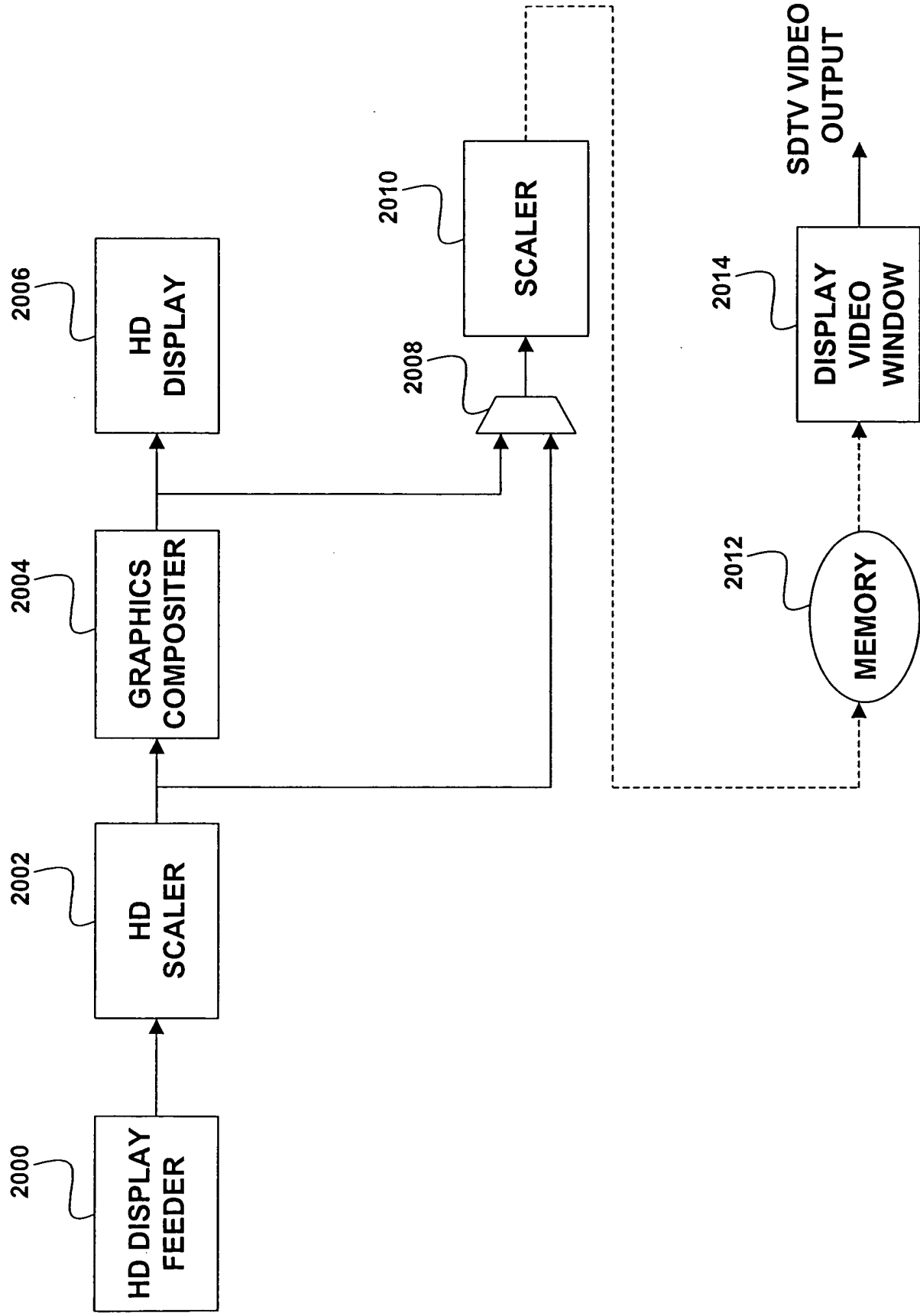


FIG. 47



**FIG. 48**



# MPEG VIDEO DECODING STAGES

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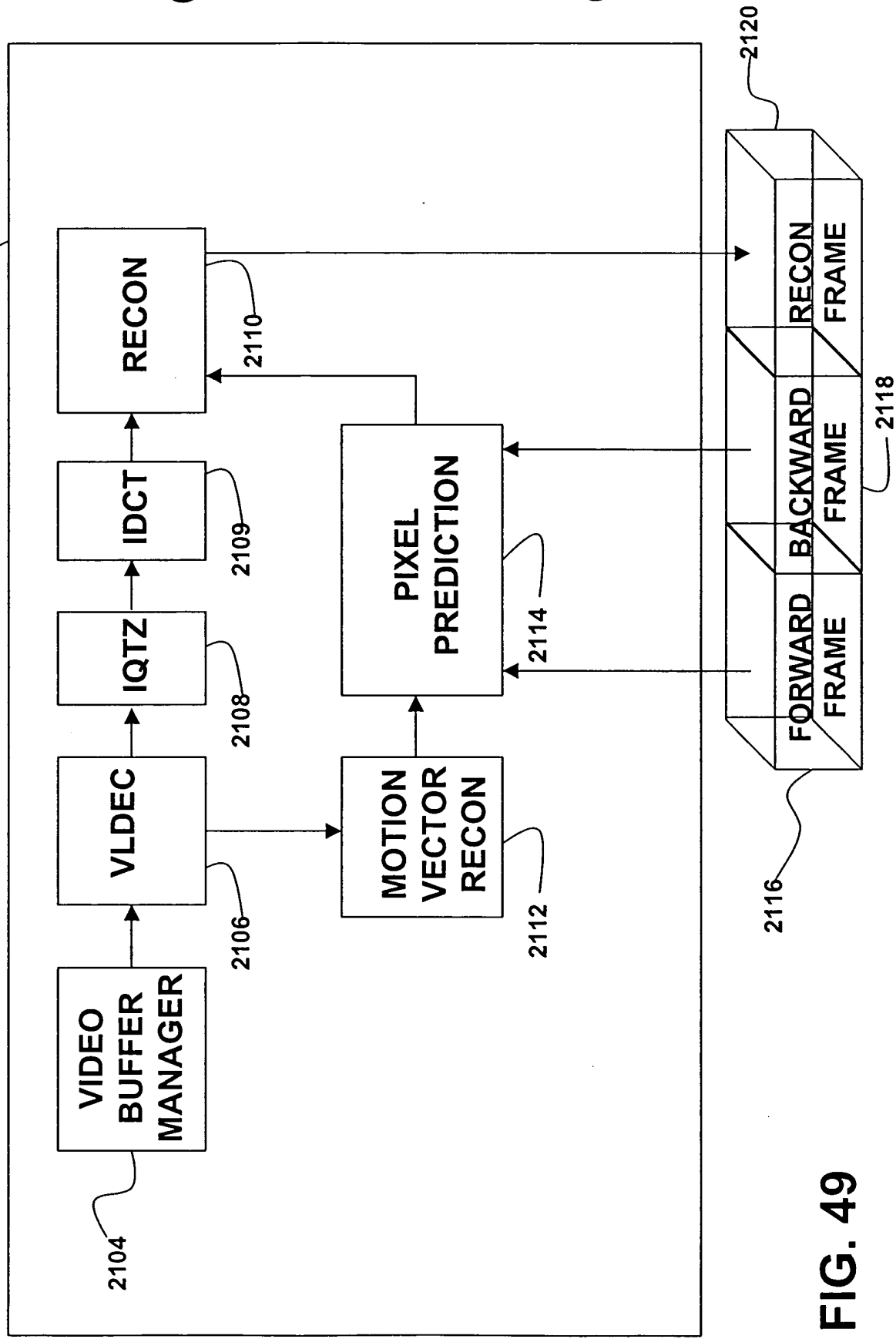
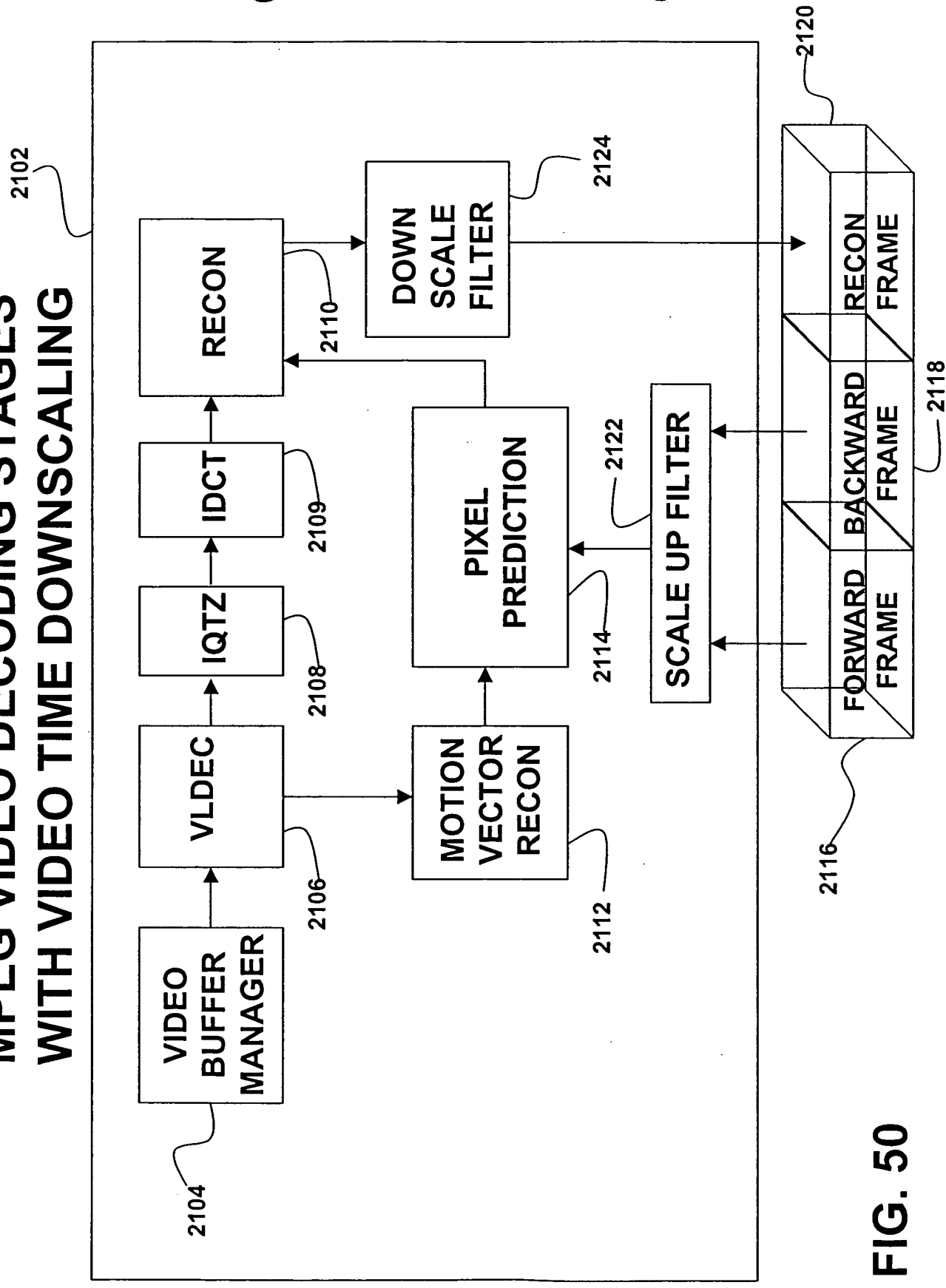


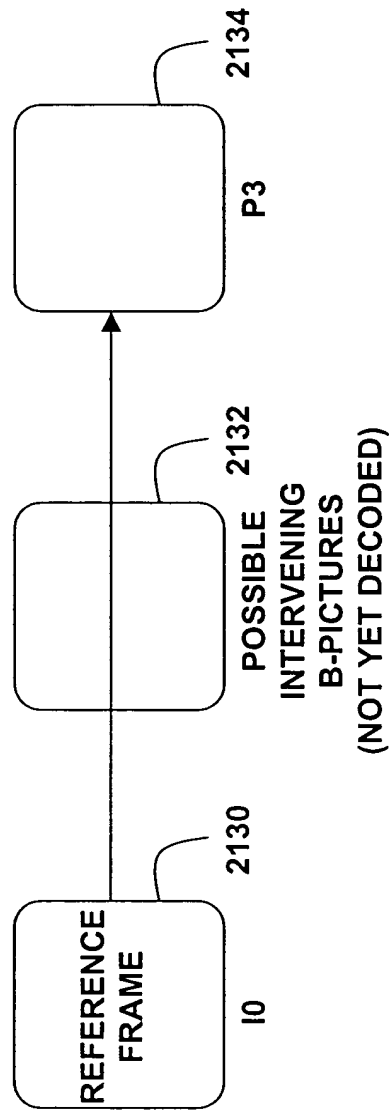
FIG. 49

# MPEG VIDEO DECODING STAGES WITH VIDEO TIME DOWNSCALING



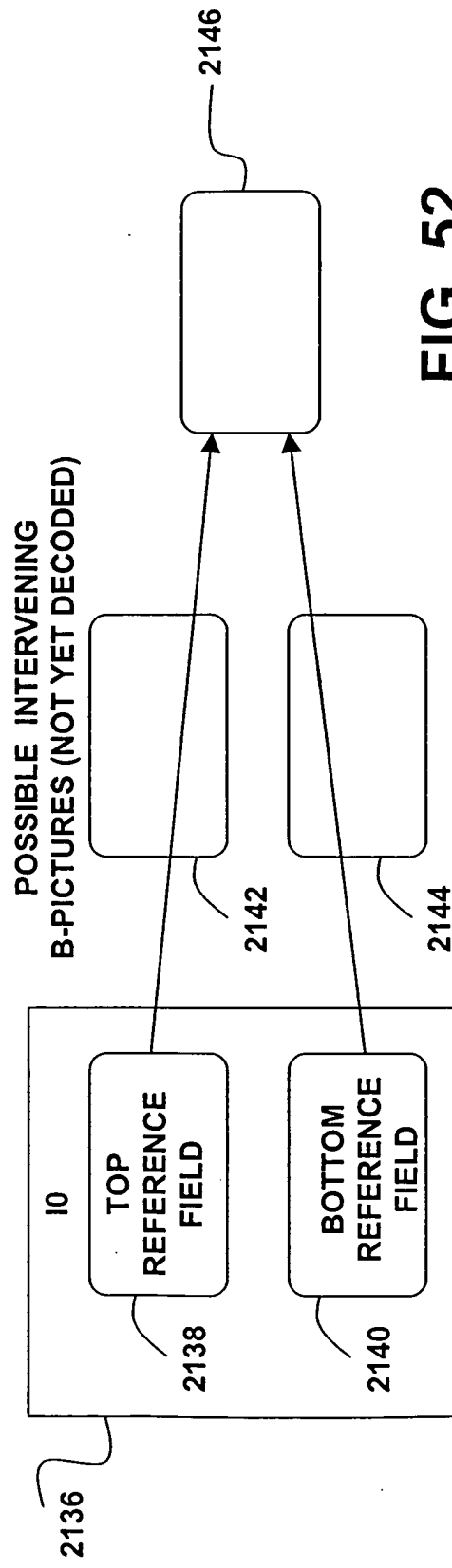
**FIG. 50**

# FRAME-PREDICTION FOR I-PICTURES AND P-PICTURES



**FIG. 51**

# FIELD PREDICTION IN A FRAME-PICTURE



**FIG. 52**

# PREDICTION OF THE FIRST FIELD-PICTURE

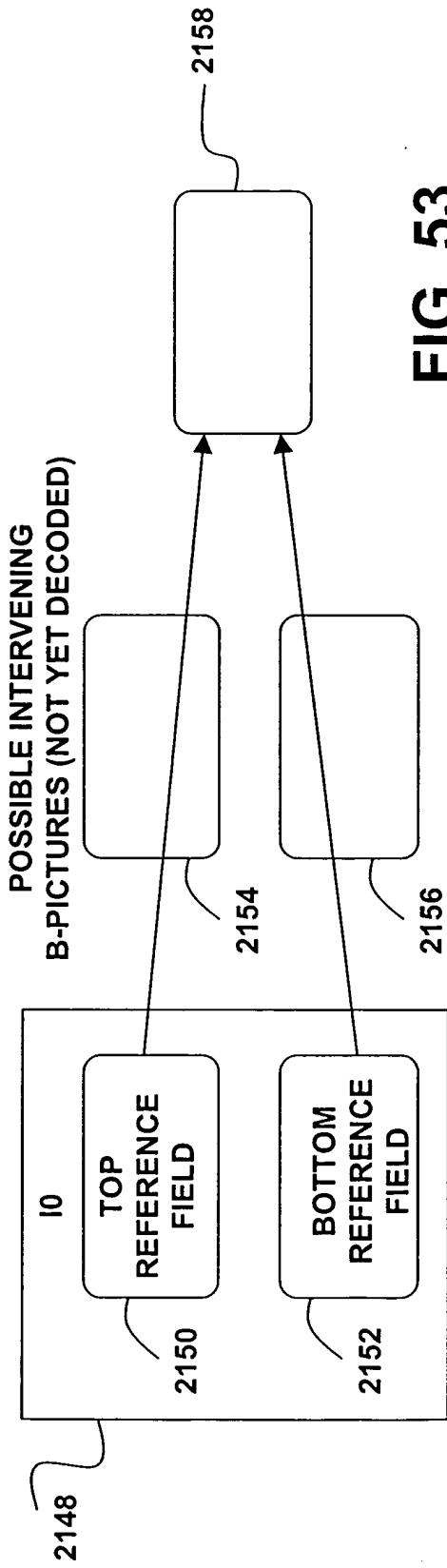


FIG. 53

# PREDICTION OF THE "BOTTOM FIELD" SECOND FIELD-PICTURE

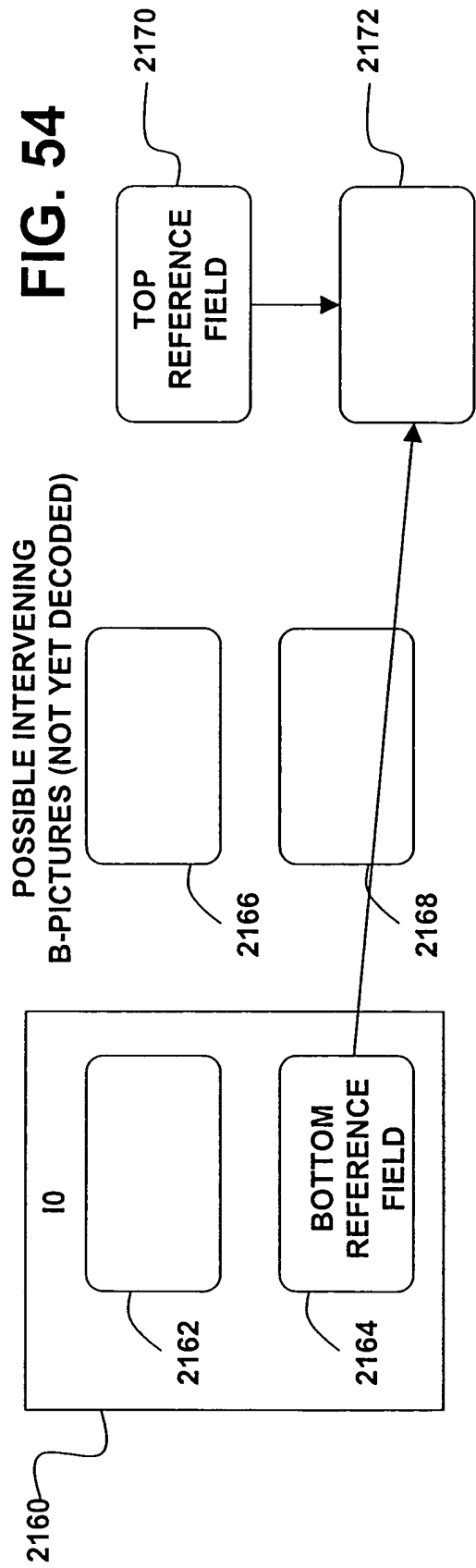


FIG. 54

# PREDICTION OF THE "TOP FIELD" SECOND FIELD-PICTURE

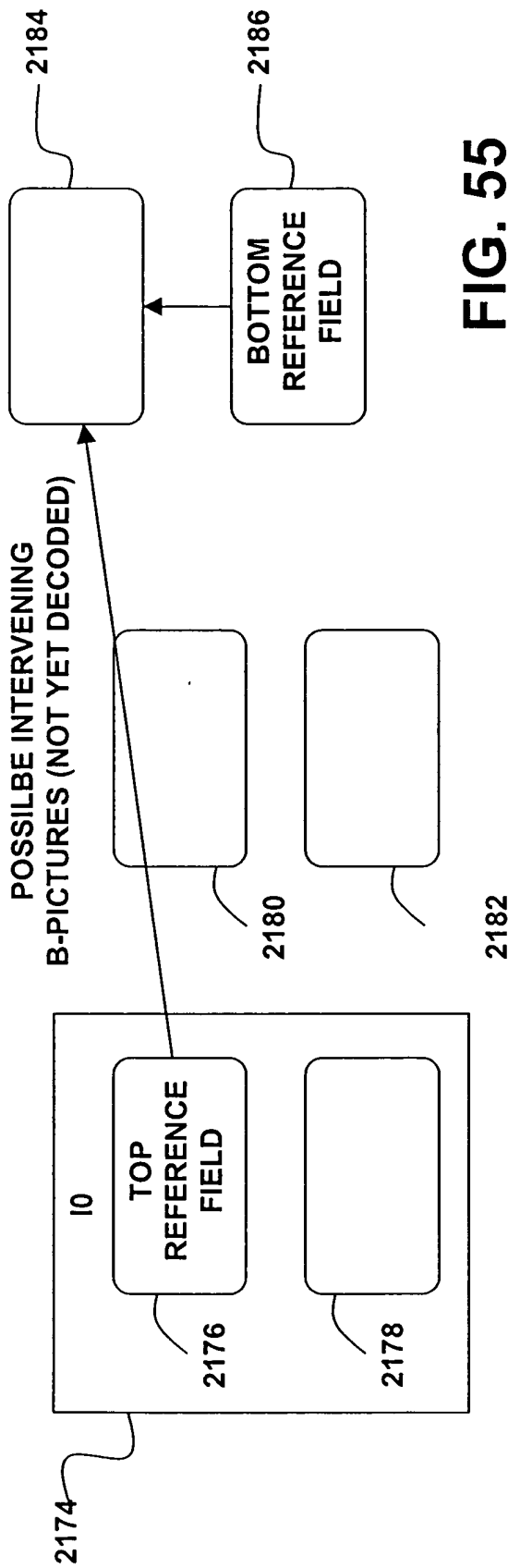


FIG. 55

# FIELD-PREDICTION OF B FIELD PICTURES OR B FRAME PICTURES

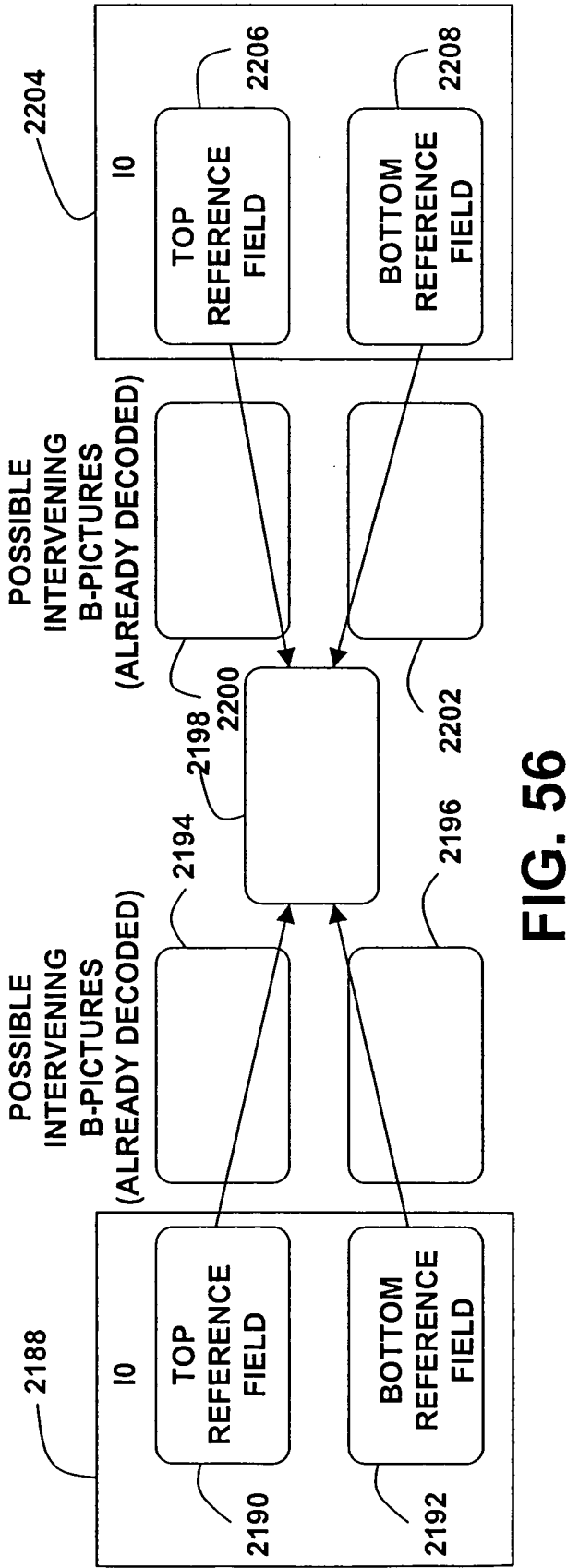


FIG. 56

# FRAME-PREDICTIONS FOR B-PICTURES

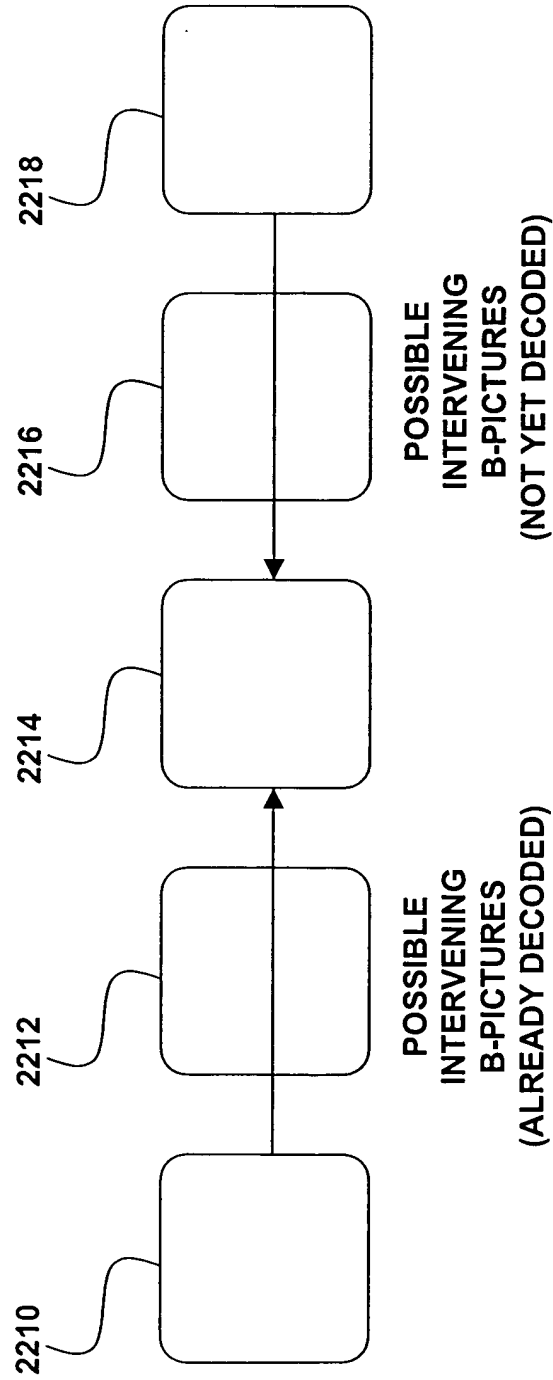


FIG. 57

# Image Organization - 64 bit SDRAM 2250

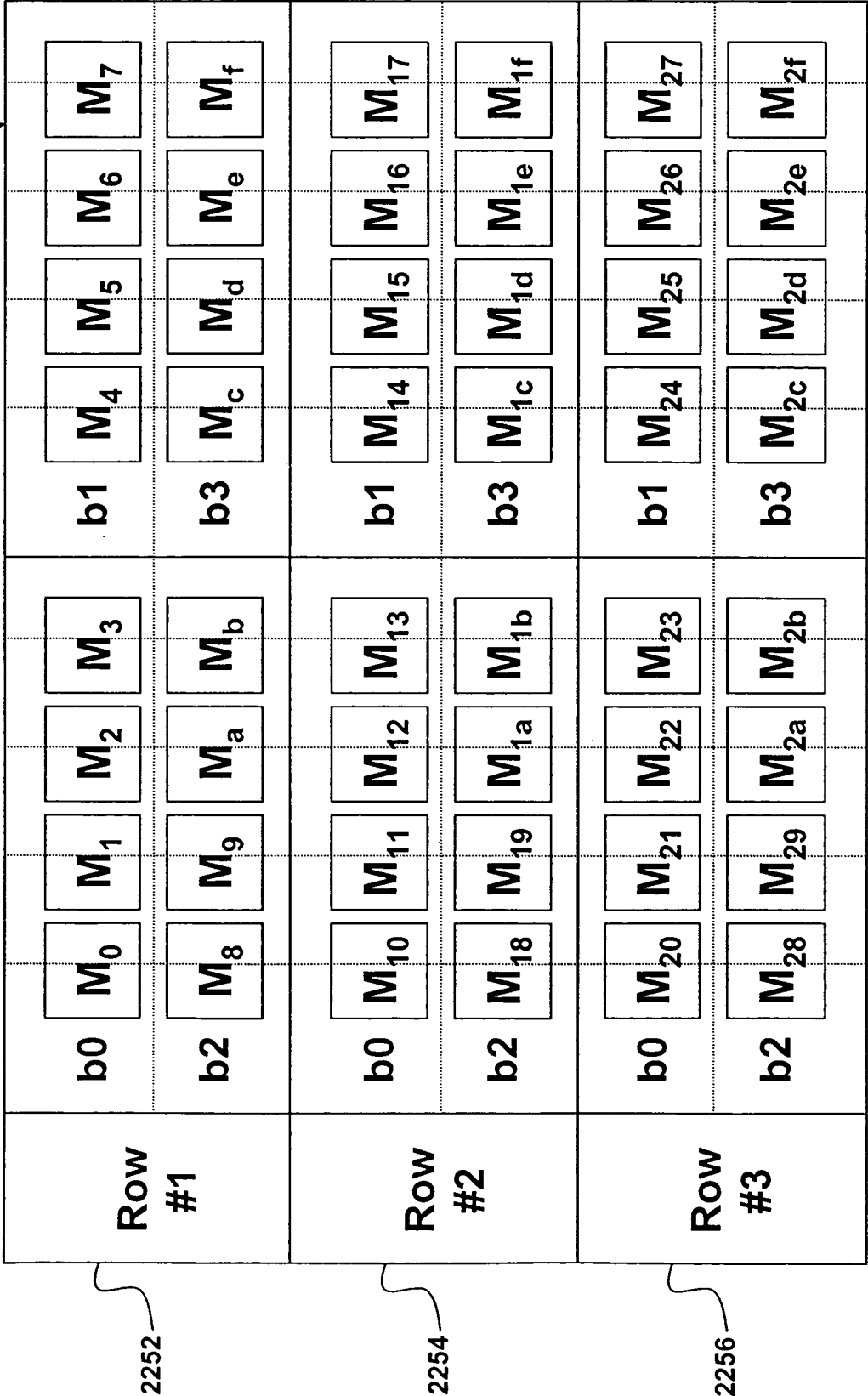


FIG. 58

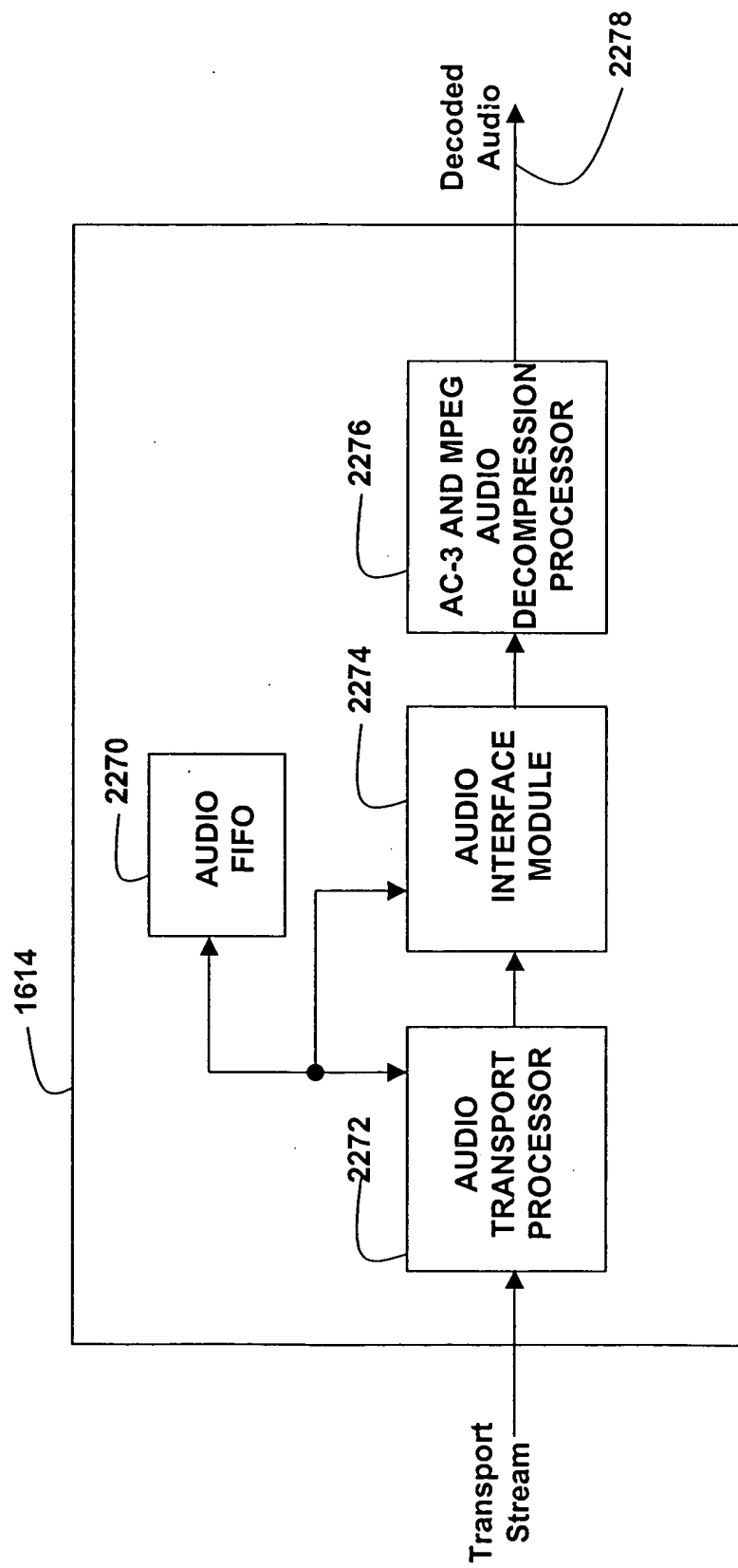


FIG. 59



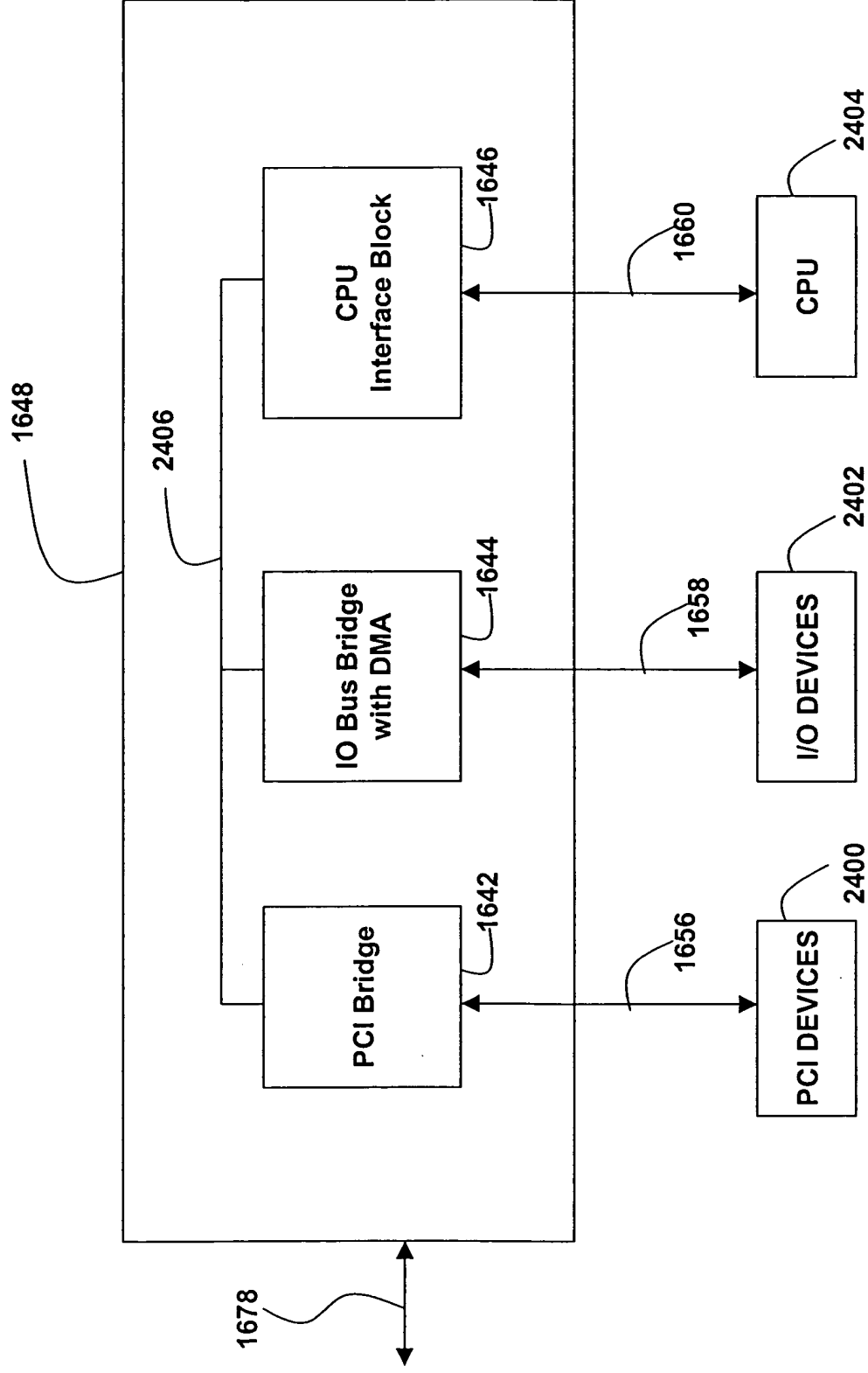
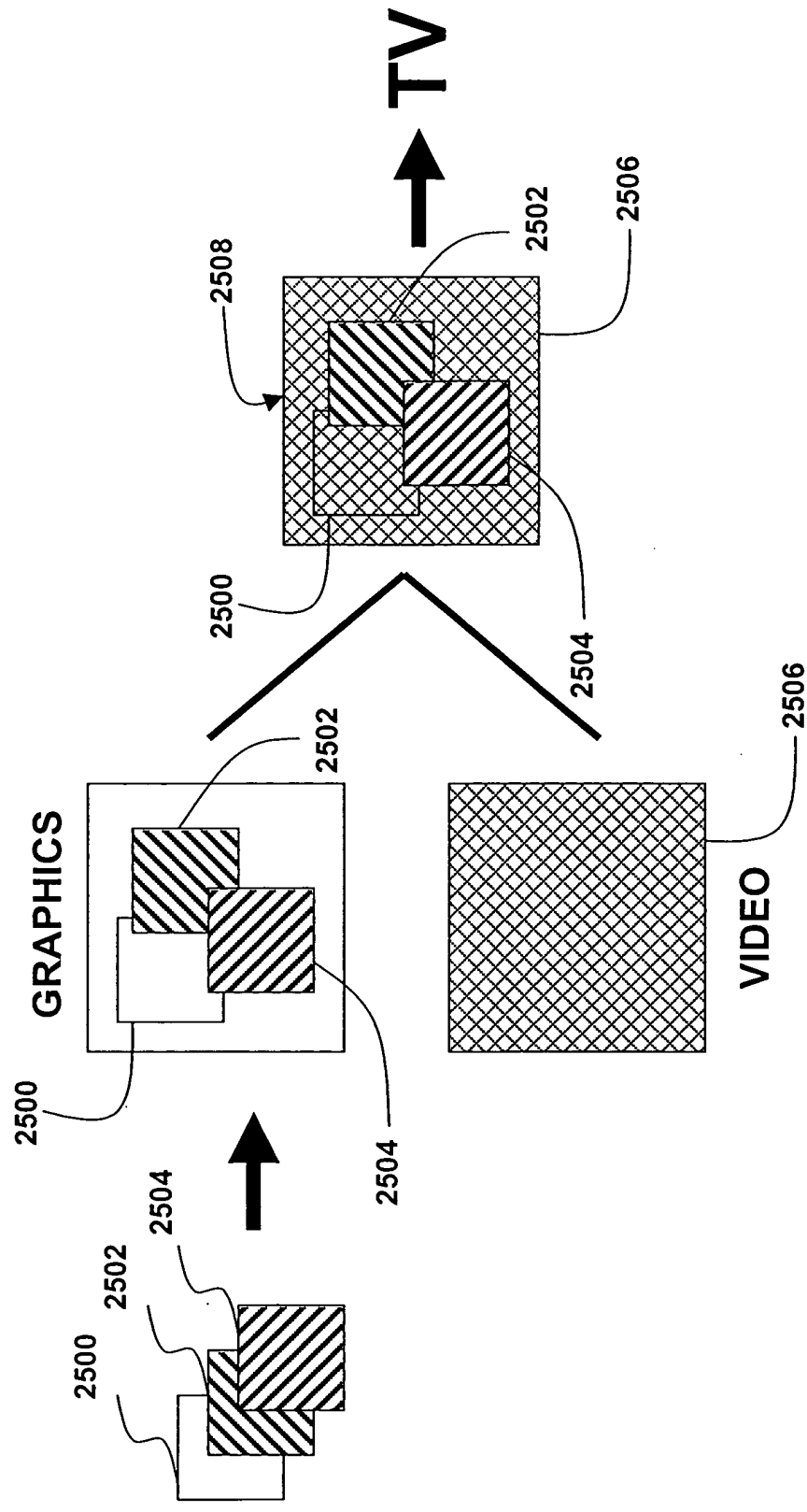


FIG. 60



**FIG. 61**

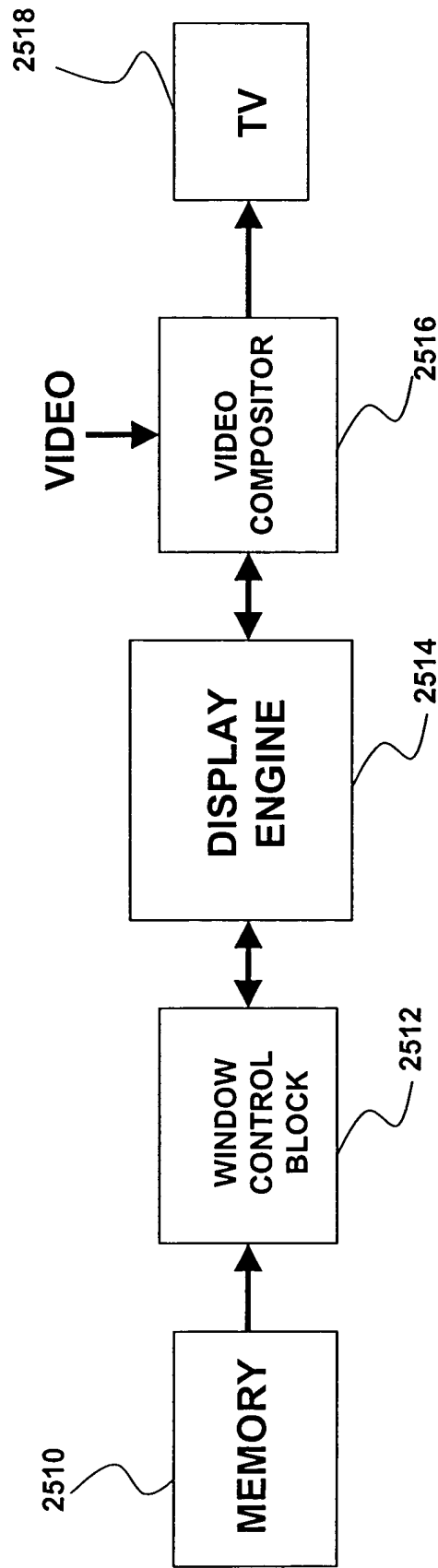


FIG. 62

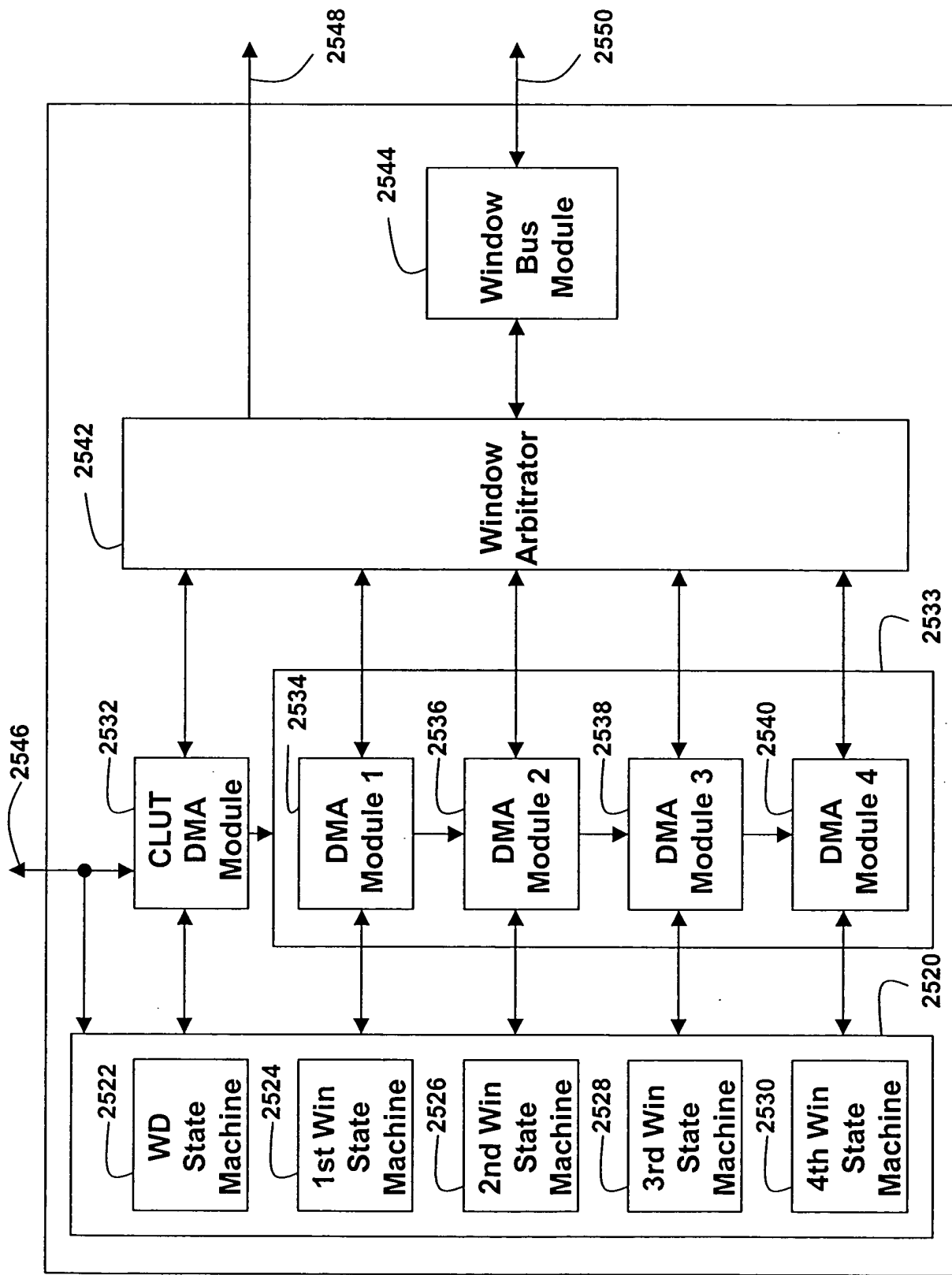


FIG. 63

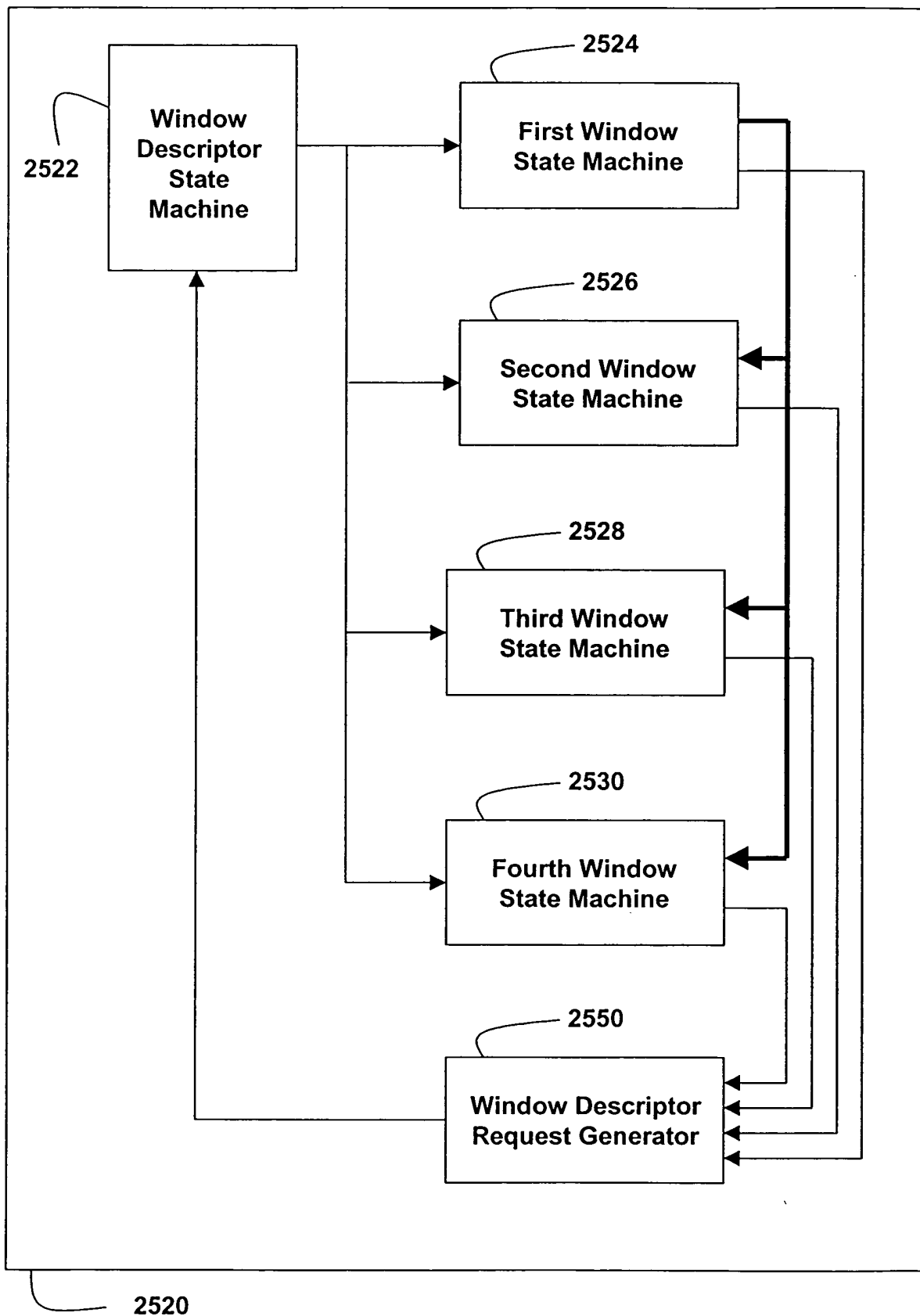


FIG. 64

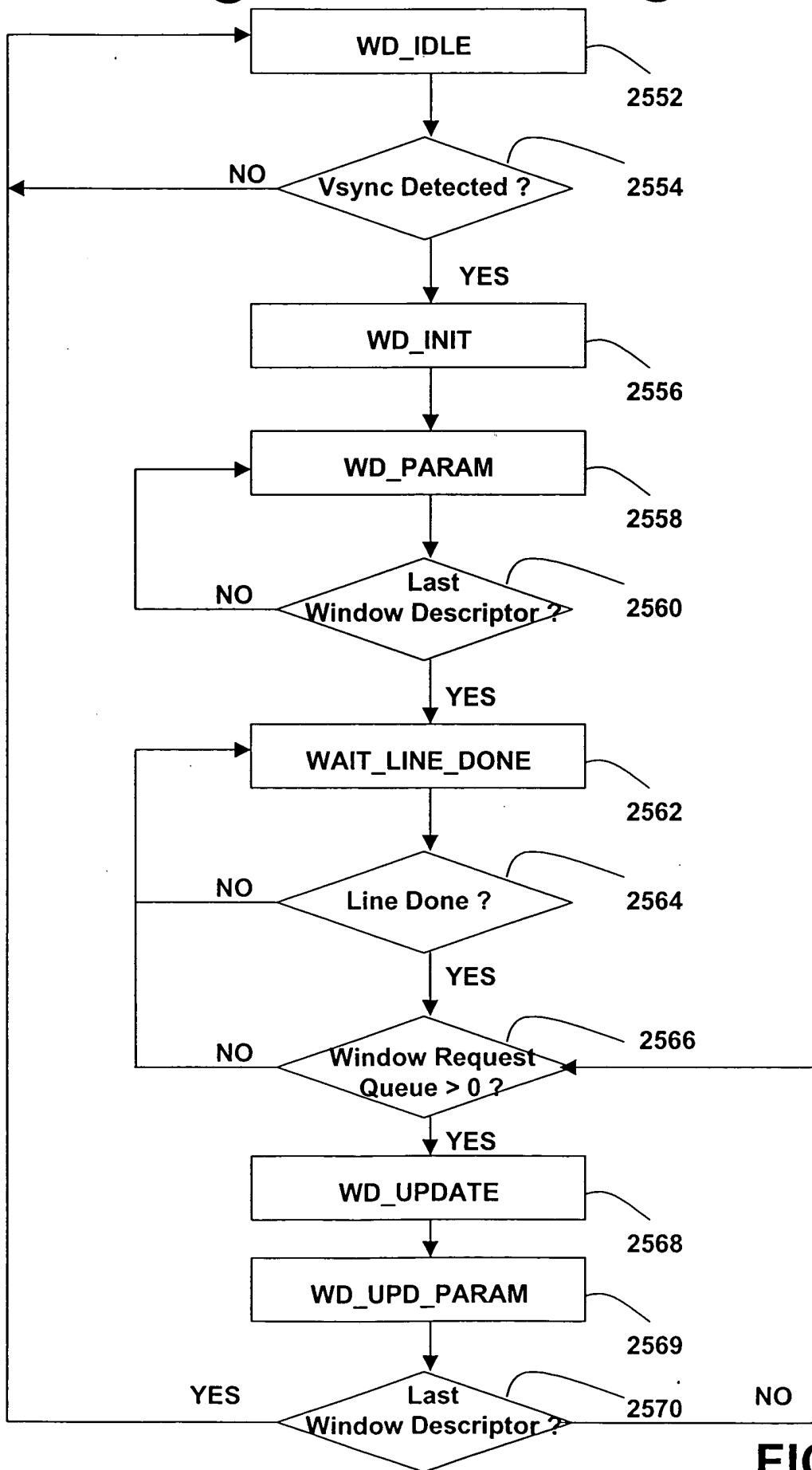
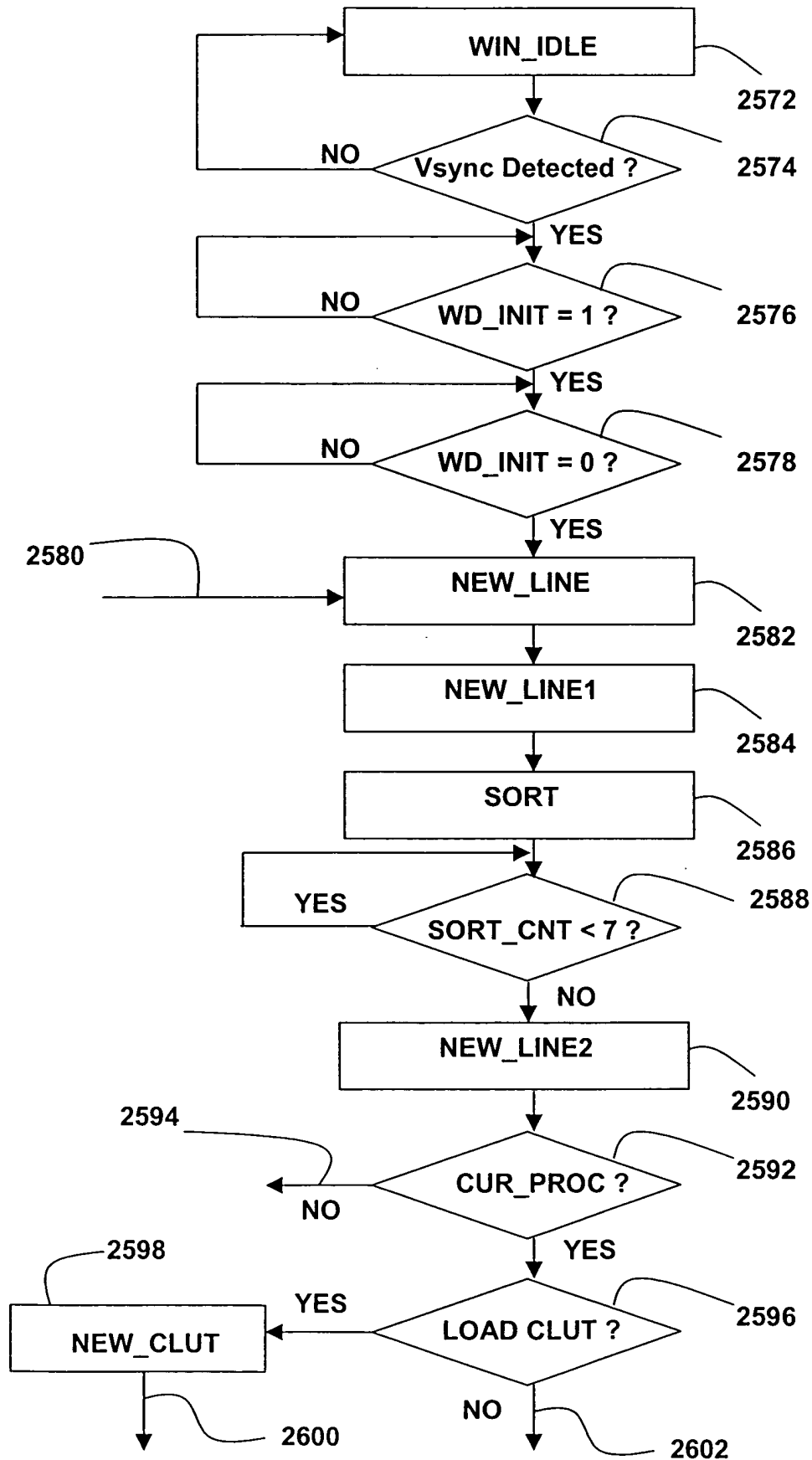


FIG. 65



**FIG. 66**

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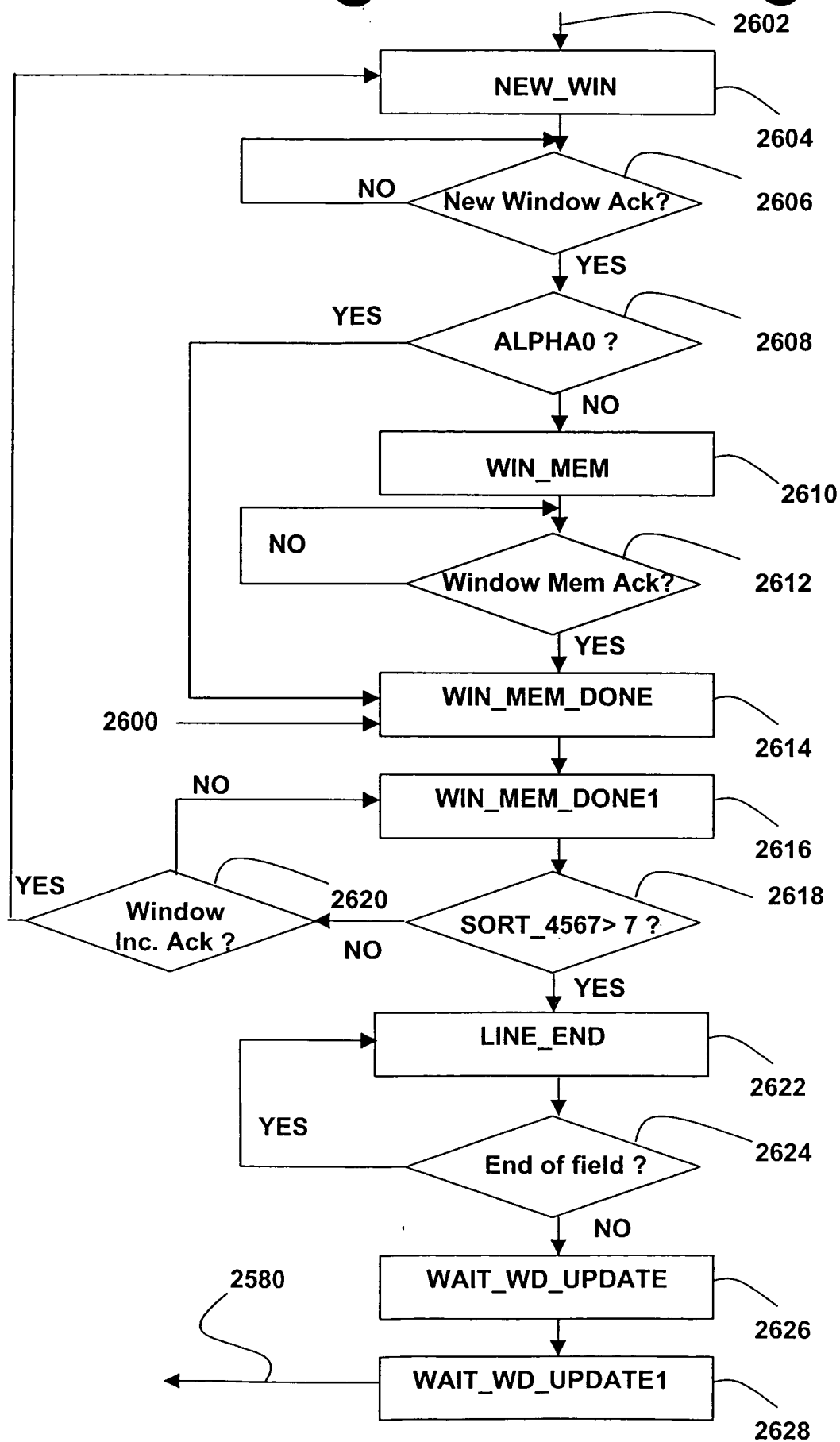
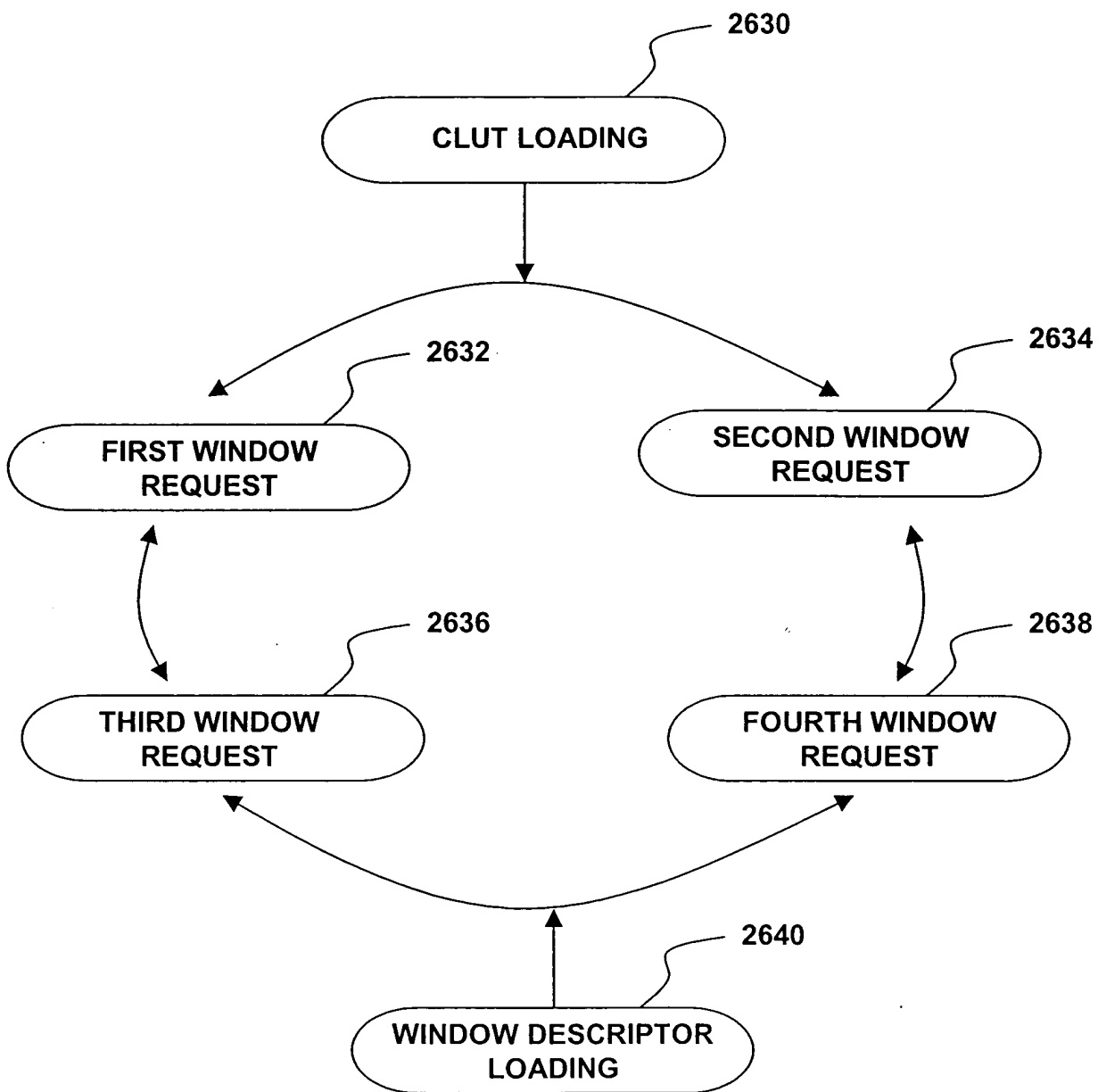


FIG. 67





**FIG. 68**

# DISPLAY ENGINE

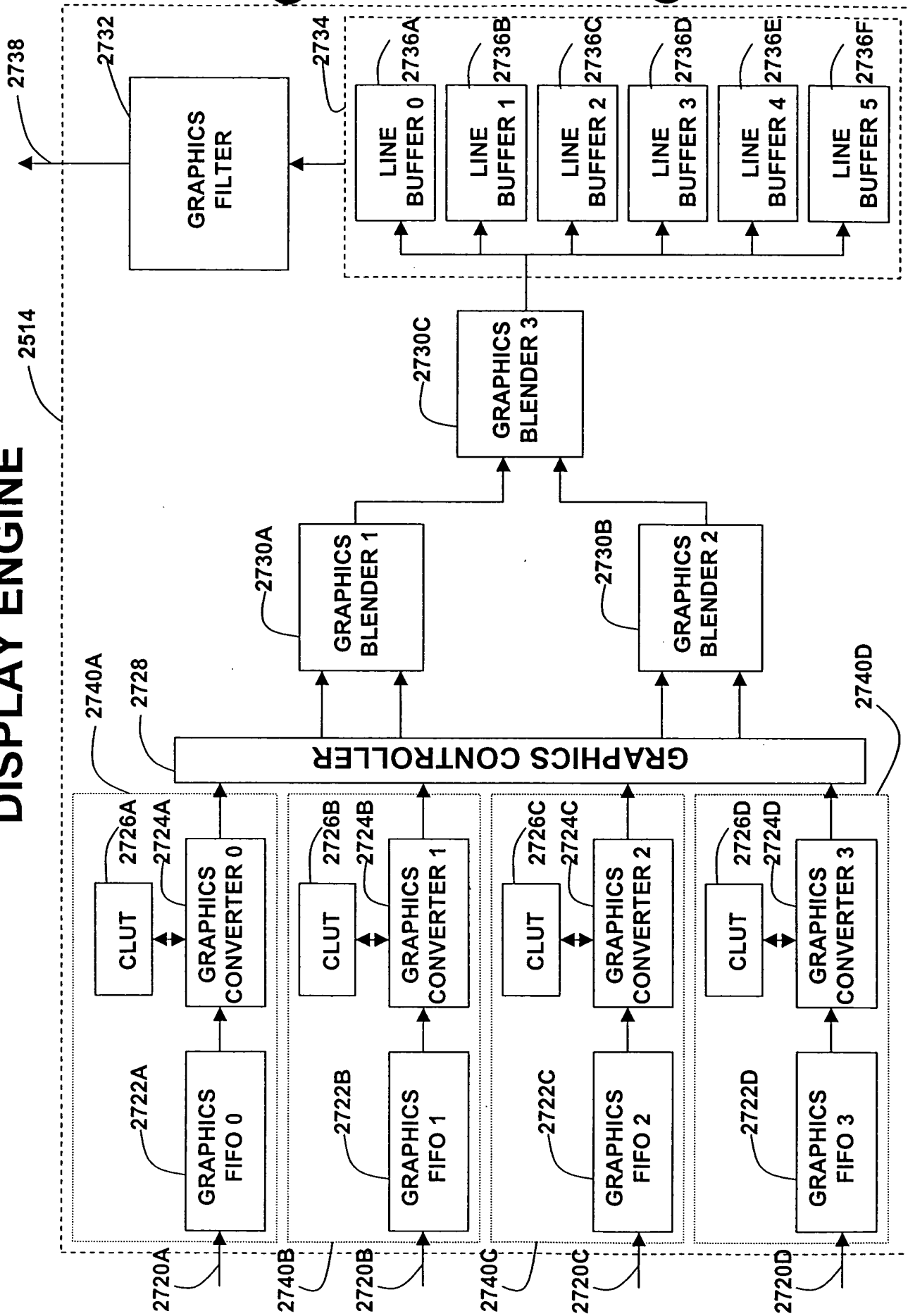
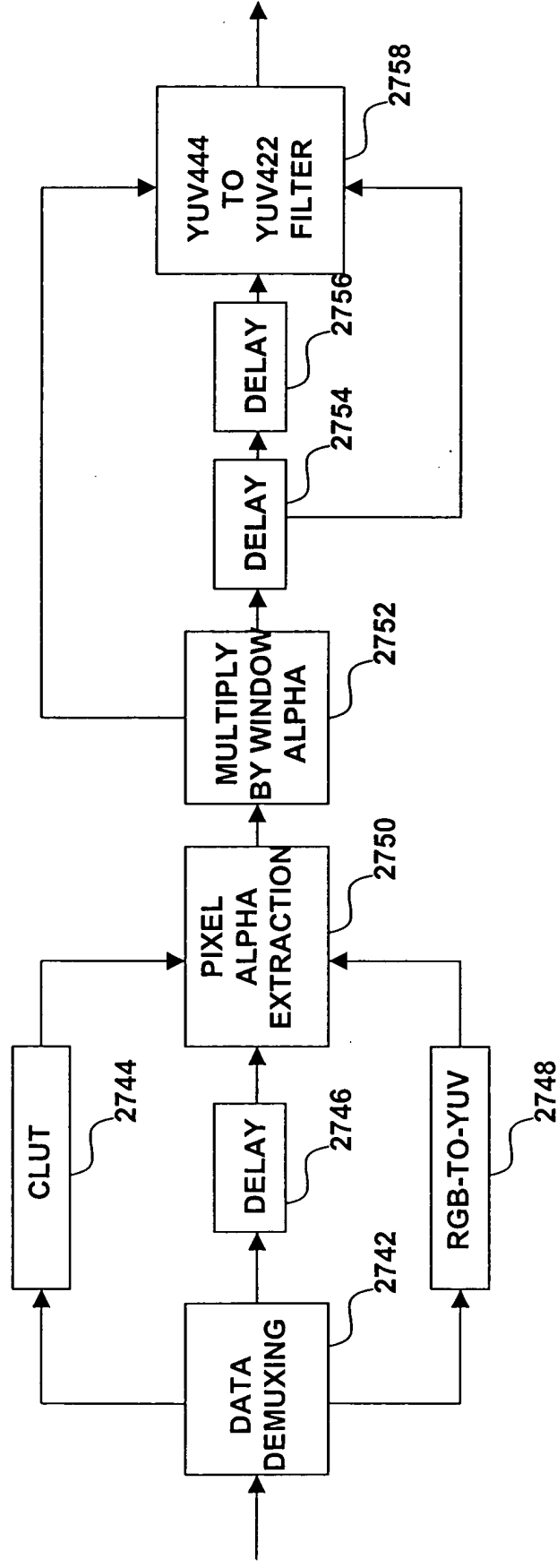


FIG. 69



**FIG. 70**

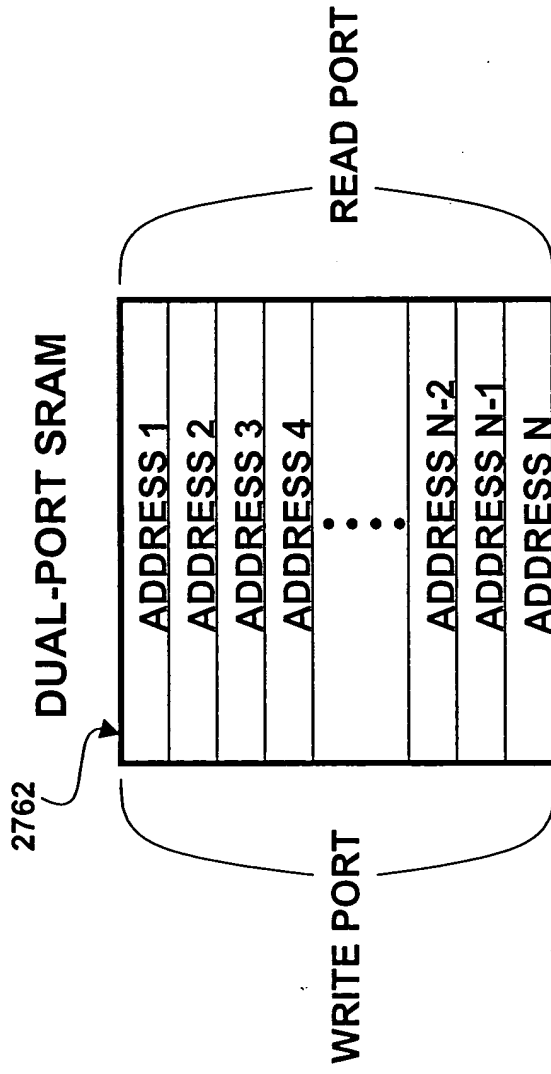


FIG. 71

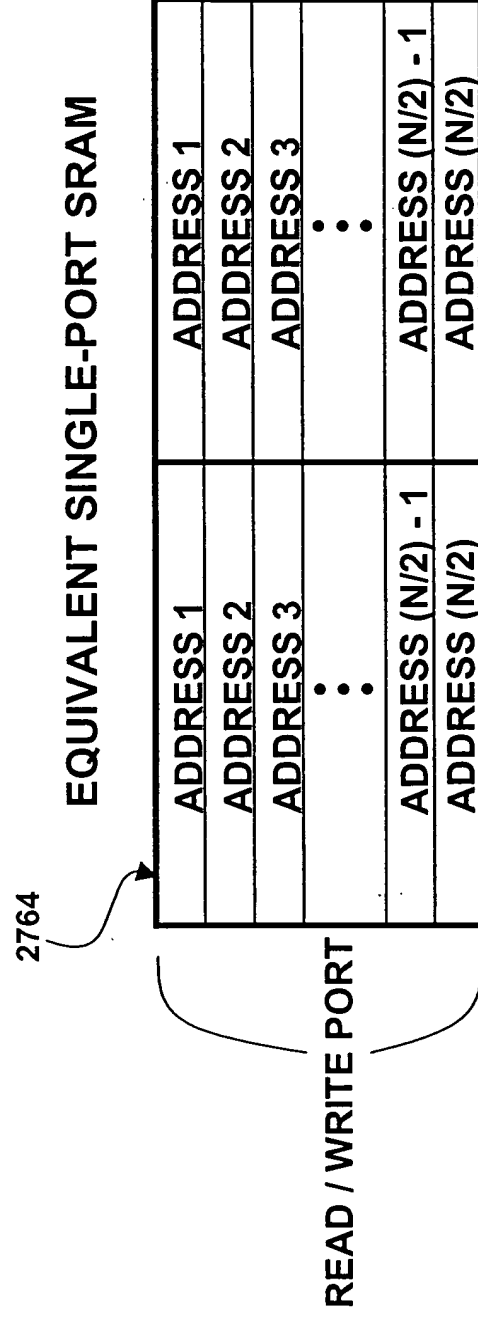


FIG. 72

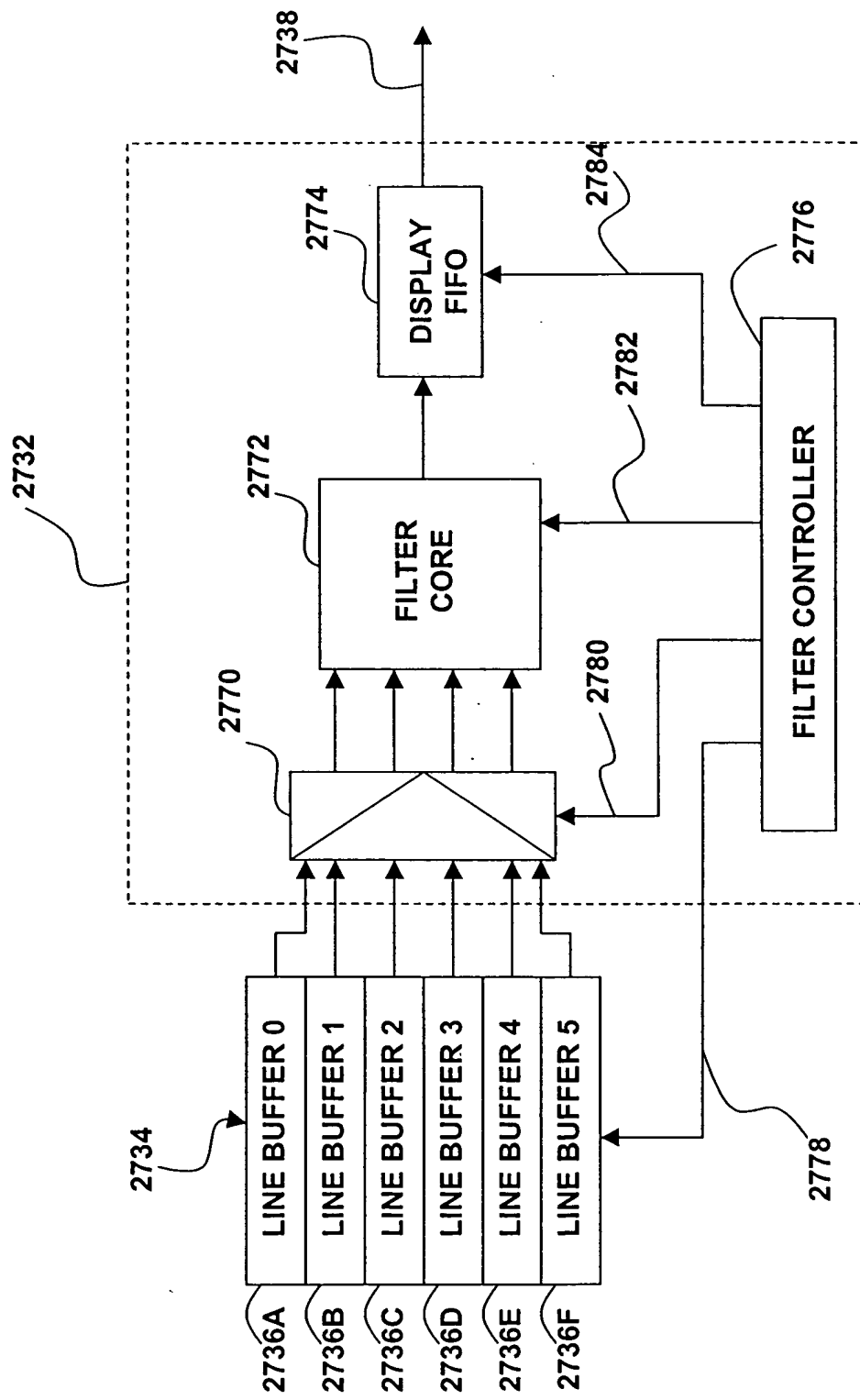


FIG. 73

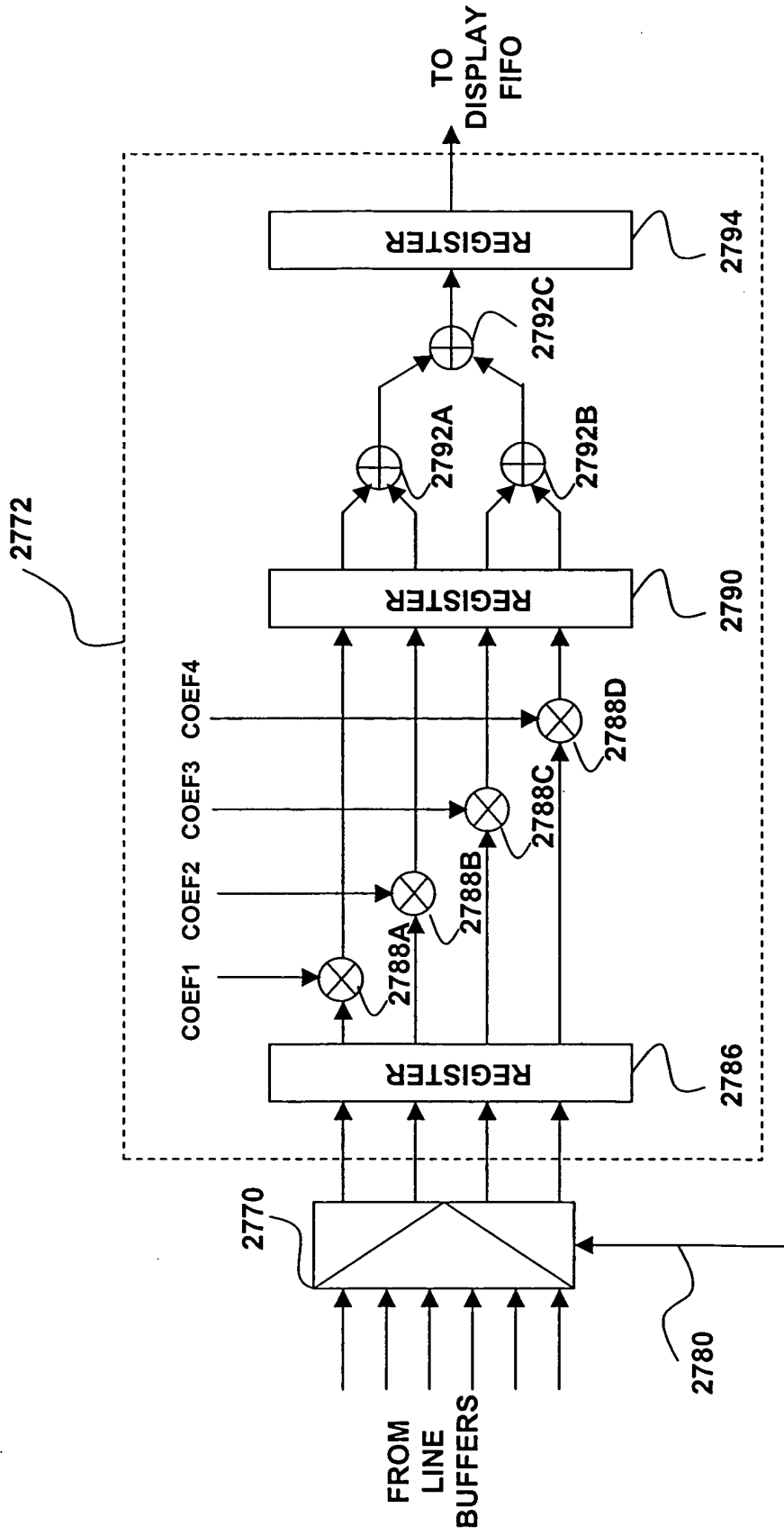


FIG. 74